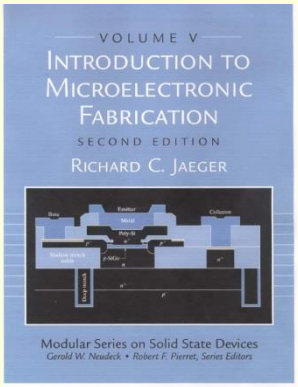
Introduction to Microelectronic Fabrication

Chapter 5
Ion Implantation



Ion Implantation

High Energy Accelerator

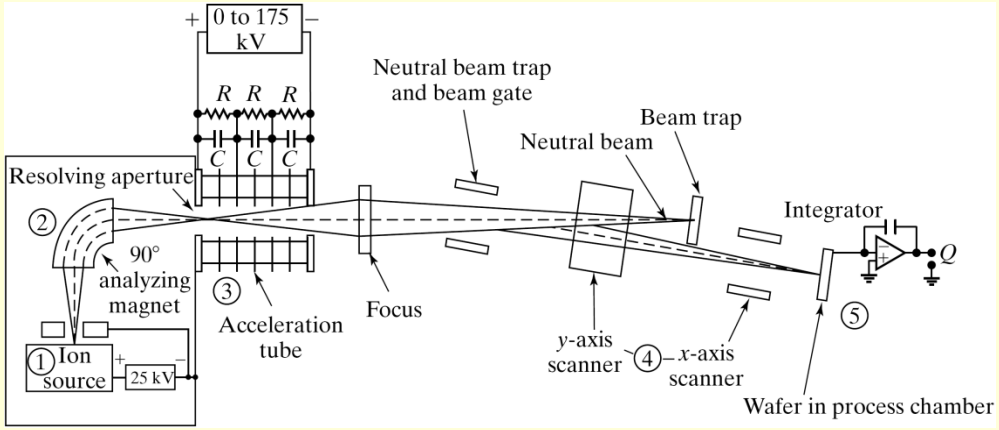


FIGURE 5.1
Schematic drawing of a typical ion implanter

1. Ion Source
2. Mass Spectrometer
3. High-Voltage Accelerator (Up to 5 MeV)
4. Scanning System
5. Target Chamber

Force on charged particle $\vec{\mathbf{F}} = q(\vec{\mathbf{v}} \times \vec{\mathbf{B}})$

Magnetic Field $|\vec{\mathbf{B}}| = \sqrt{\frac{2mV}{qr^2}}$

Implanted Dose $Q = \frac{1}{mqA}\int_0^T I(t)dt$

m = mass

$\vec{\mathbf{v}}$ = velocity

V = acceleration potential

A = wafer area

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

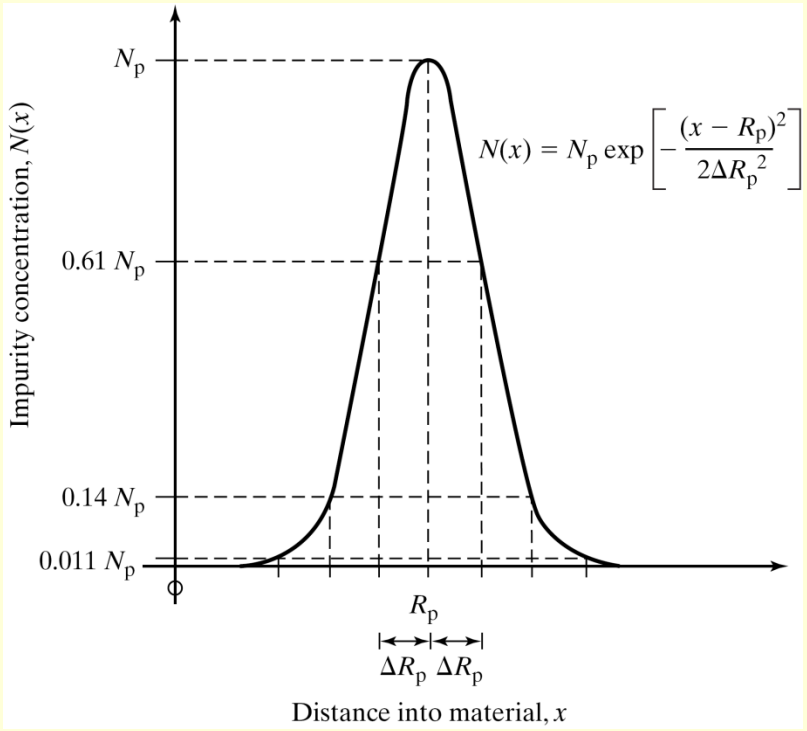
Ion Implantation
Overview

- Wafer is Target in High Energy Accelerator
- Impurities “Shot” into Wafer
- Preferred Method of Adding Impurities to Wafers
  - Wide Range of Impurity Species (Almost Anything)
  - Tight Dose Control (A few % vs. 20-30% for high temperature pre-deposition processes)
  - Low Temperature Process
- Expensive Systems
- Vacuum System

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Ion Implantation

Mathematical Model



Gaussian Profile

$$N(x) = N_p \exp\left[-\frac{(x - R_p)^2}{2\Delta R_p^2}\right]$$

R_p = Projected Range

ΔR_p = Straggle

Dose $$Q = \int_0^\infty N(x)dx = \sqrt{2\pi} N_p \Delta R_p$$

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Ion Implantation
Projected Range

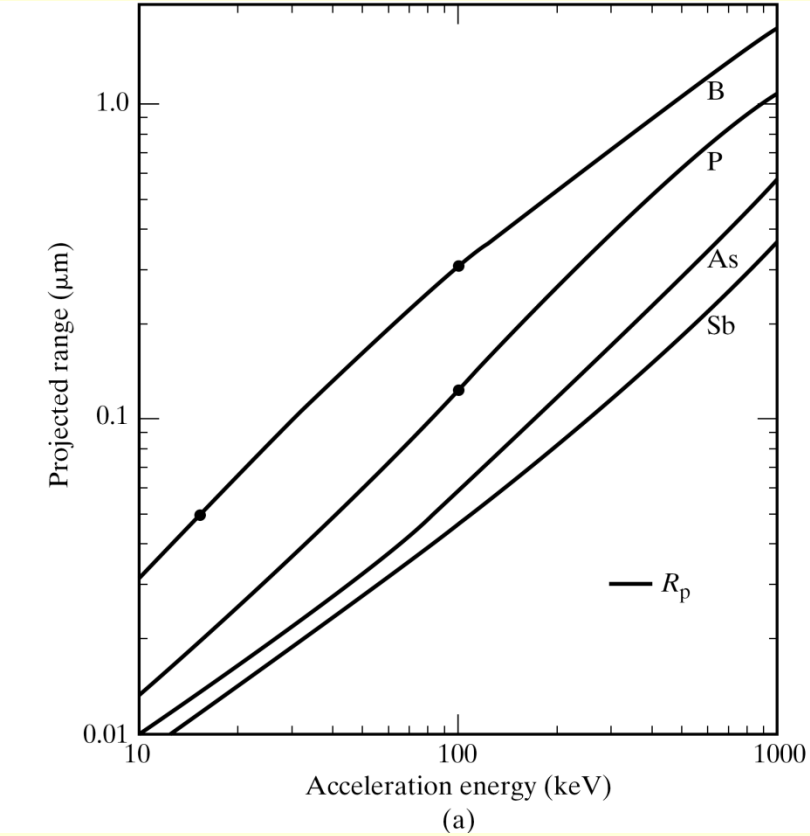


FIGURE 5.3

Projected range and straggle calculations based on LSS theory. (a) Projected range $R_{p\_}$ for boron, phosphorus, arsenic, and antimony in amorphous silicon. Results for SiO_2 and for silicon are virtually identical. (b) Vertical $\_R_p$ and transverse $\_R_l$ straggle for boron, phosphorus, arsenic, and antimony. Reprinted with permission from Ref. [2]. (Copyright van Nostrand Reinhold Company, Inc.)

Ion Implantation
Straggle

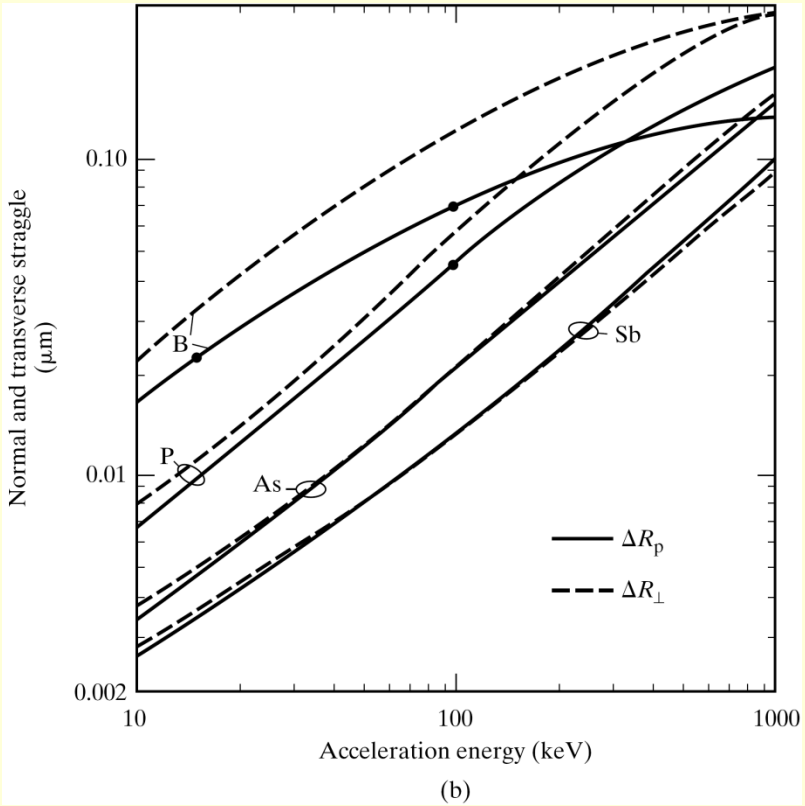
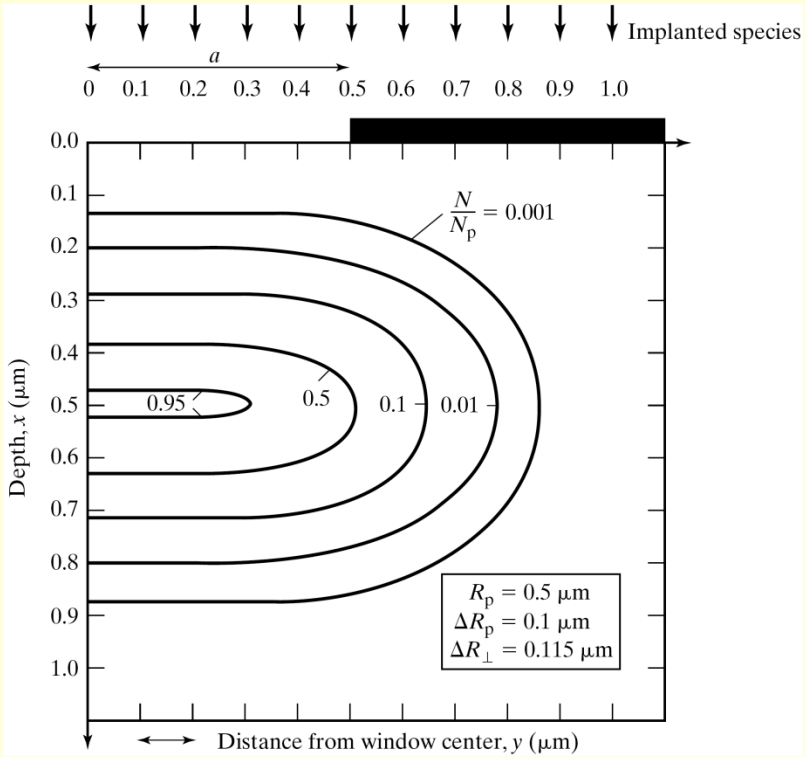


FIGURE 5.3

Projected range and straggle calculations based on LSS theory. (a) Projected range $R_{p\_}$ for boron, phosphorus, arsenic, and antimony in amorphous silicon. Results for SiO_2 and for silicon are virtually identical. (b) Vertical $\_R_p$ and transverse $\_R_l$ straggle for boron, phosphorus, arsenic, and antimony. Reprinted with permission from Ref. [2]. (Copyright van Nostrand Reinhold Company, Inc.)

Ion Implantation
Selective Implantation



$$N(x,y) = N(x)F(y)$$

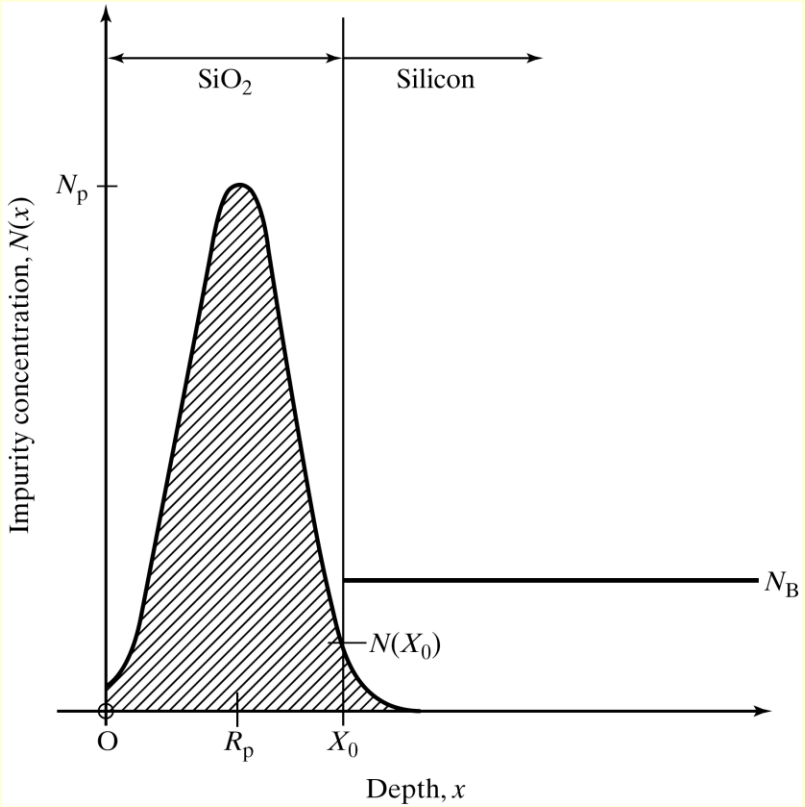
$$F(y) = \frac{1}{2}\left[erfc\left(\frac{y-a}{\sqrt{2}\Delta R_{\perp}}\right) - erfc\left(\frac{y+a}{\sqrt{2}\Delta R_{\perp}}\right)\right]$$

$\Delta R_{\perp}$ = transverse straggle

N(x) is one - dimensional solution

Figure 5.4
Contours of equal ion concentration for an implantation into silicon through a 1-μm window. The profiles are symmetrical about the x-axis and were calculated using the equation above taken from Ref. [3].

Ion Implantation
Selective Implantation



- Desire Implanted Impurity Level to be Much Less Than Wafer Doping

$$N(X_0) << N_B$$

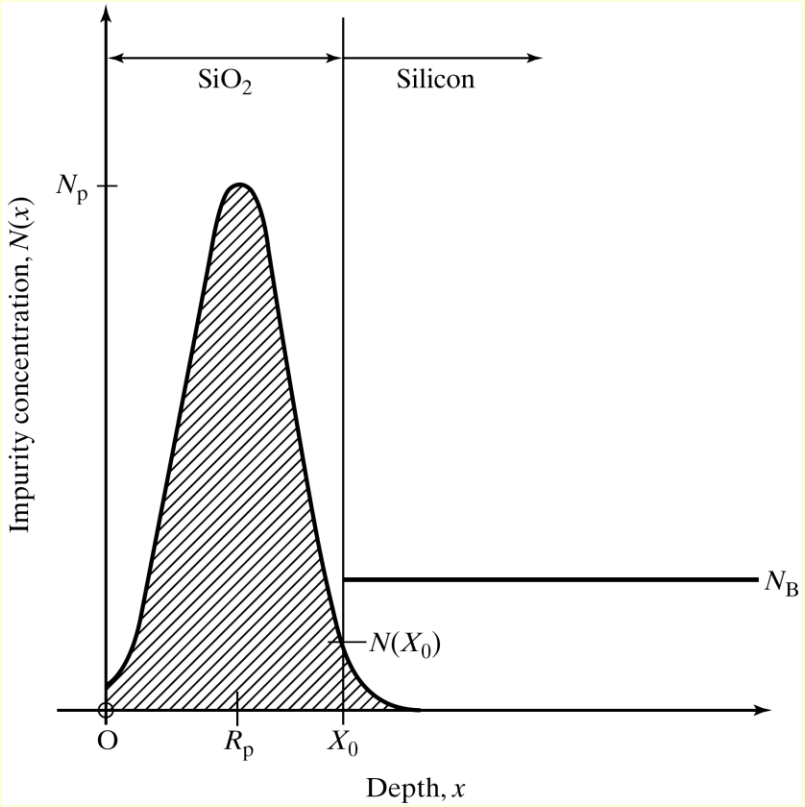
or

$$N(X_0) < N_B/10$$

FIGURE 5.5

Implanted impurity profile with implant peak in the oxide. The barrier material must be thick enough to ensure that the concentration in the tail of the distribution is much less than N_B.

Ion Implantation
Selective Implantation

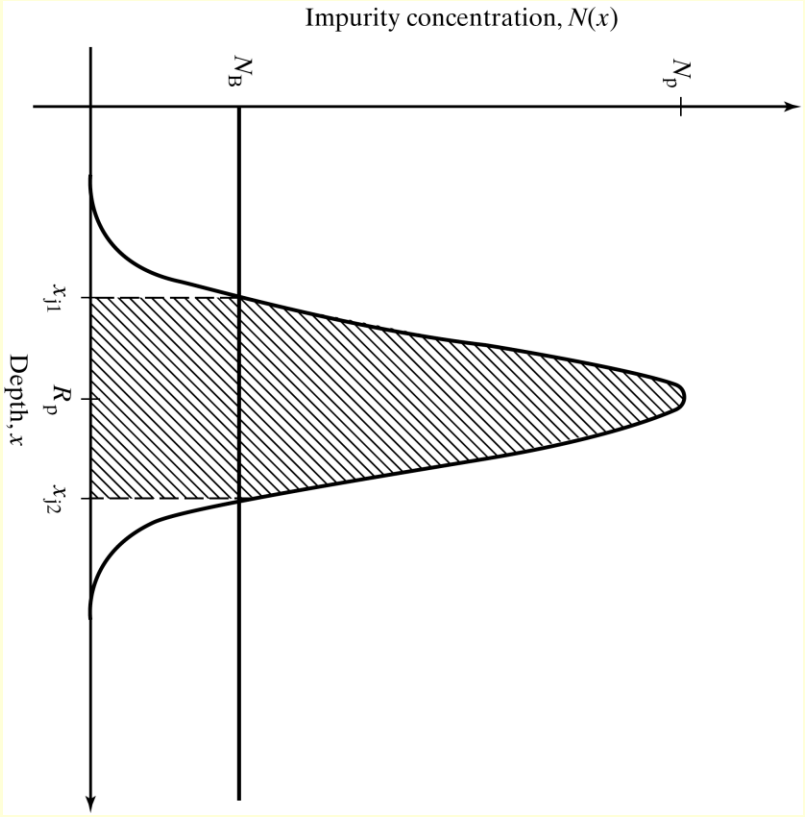


$$X_0 \geq R_p + \Delta R_p \sqrt{2 \ln\left(\frac{10 N_p}{N_B}\right)} = R_p + m \Delta R_p$$

TABLE 5.1 Values of m for Various Values of N_p/N_B.

N_p/N_B	m
10^1	3.0
10^2	3.7
10^3	4.3
10^4	4.8
10^5	5.3
10^6	5.7

Ion Implantation
Junction Depth



$$N(x_j) = N_B$$

$$N_p \exp\left[-\frac{(x_j - R_p)^2}{2\Delta R_p^2}\right] = N_B$$

$$x_j = R_p \pm \Delta R_p \sqrt{2 \ln\left(\frac{N_p}{N_B}\right)}$$

FIGURE 5.6

Junction formation by impurity implantation in silicon. Two *pn* junctions are formed at x_{j1} and x_{j2}.

Ion Implantation
Channeling

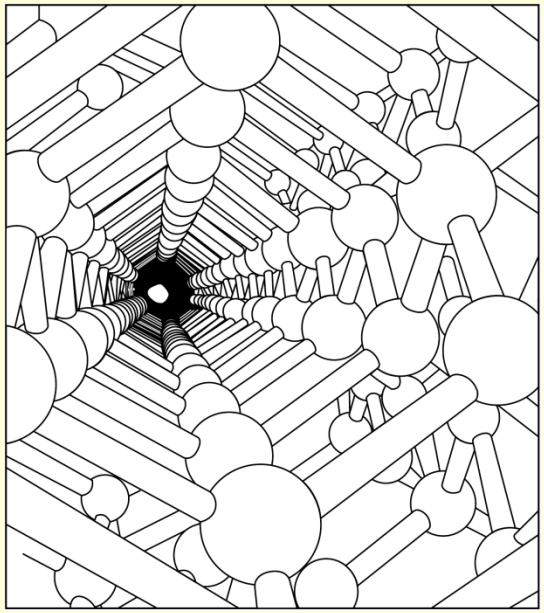


FIGURE 5.7

The silicon lattice viewed along the {110} axis. From THE ARCHITECTURE OF MOLECULES by Linus Pauling and Roger Hayward. Copyright © 1964 W. H. Freeman and Company. Reprinted with permission from Refs. [4a] and [4b].

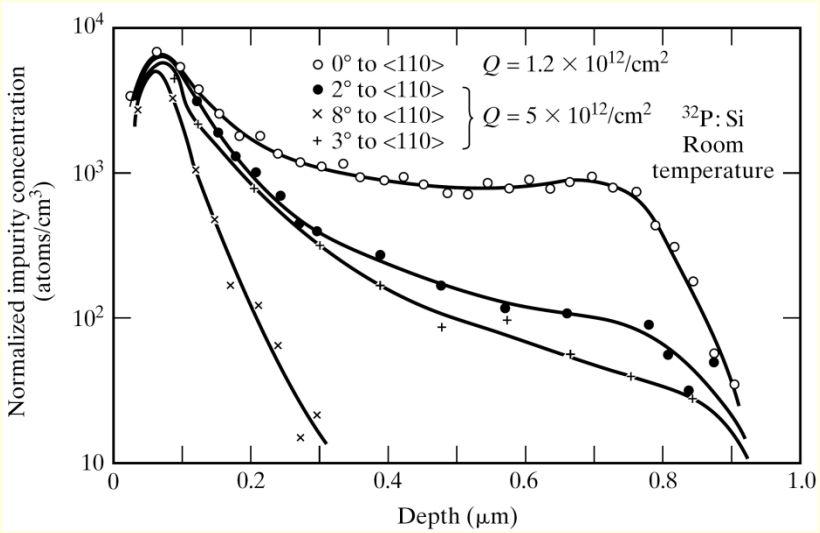
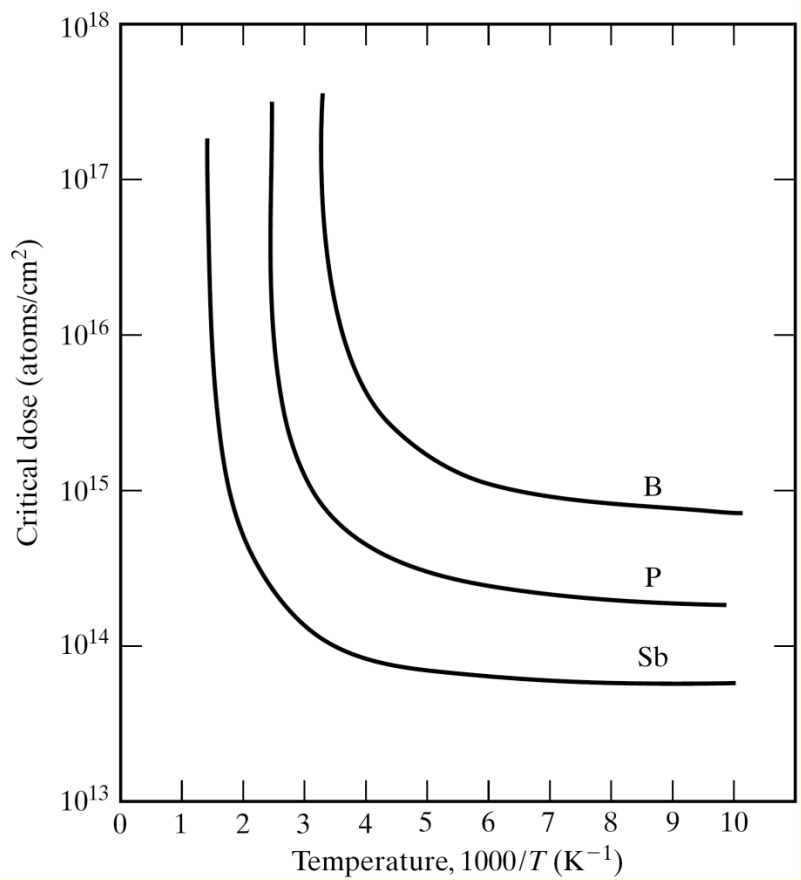


FIGURE 5.8

Phosphorus impurity profiles for 40-keV implantations at various angles from the axis. Copyright 1968 by national Research Council of Canada. Reprinted with permission from Ref. [5].

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Ion Implantation
Lattice Damage and Annealing



- Implantation Causes Damage to Surface
- Typically Removed by Annealing Cycle 800-1000^o C for 30 min.
- Rapid Thermal Annealing (RTA) Now Used for Lower Dt Product

FIGURE 5.9

A plot of the dose required to form an amorphous layer on silicon versus reciprocal target temperature. Arsenic falls between phosphorus and antimony. Copyright 1970 by Plenum Publishing Corporation. Reprinted with permission from Ref. [6].

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Ion Implantation
Deviation from Gaussian Theory

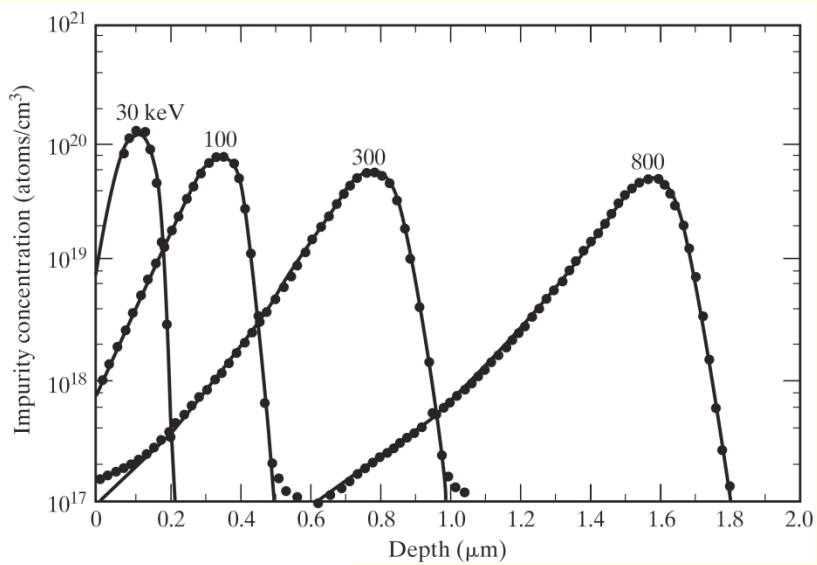
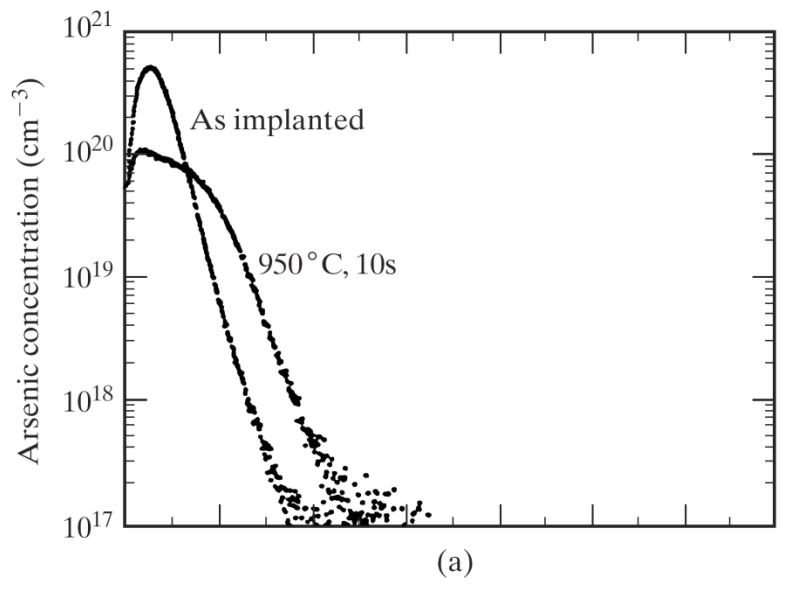


FIGURE 5.10

Measured boron impurity distributions compared with four-moment (Pearson IV) distribution functions. The boron was implanted into amorphous silicon without annealing. Reprinted with permission from Philips Journal of Research [8].

- Curves Deviate from Gaussian for Deeper Implantations (> 200 keV
- Curves Fit Four-Moment (Pearson Type-IV) Distribution Functions

Ion Implantation
Shallow Implantation



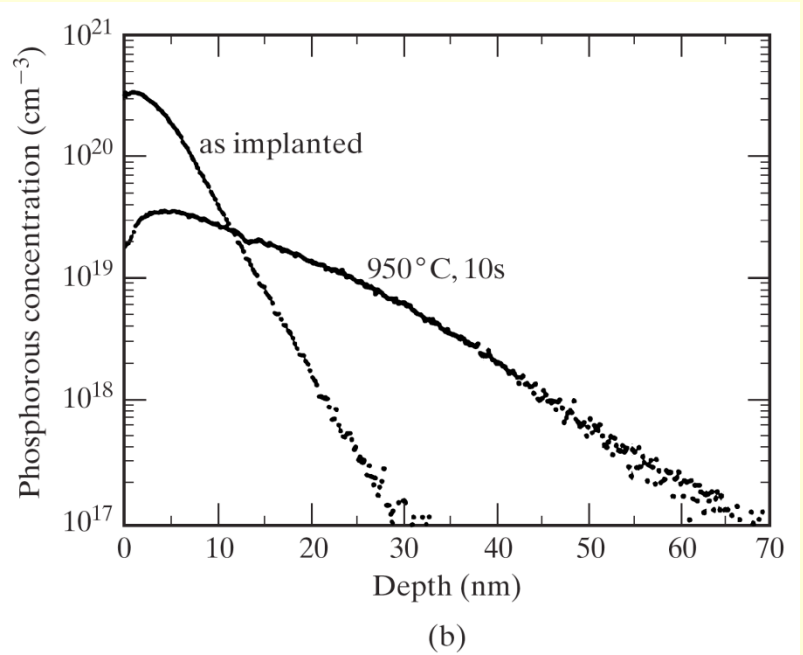
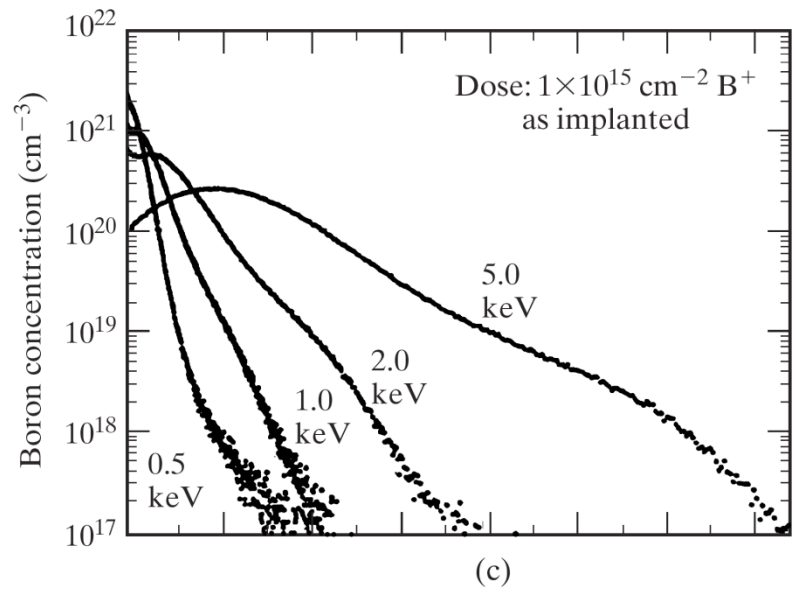


FIGURE 5.11

Examples of transient enhanced diffusion. SIMS data comparing as-implanted and annealed depth profiles from (a) 3 x $10^{14}/cm^2$, 2 keV As^+, and (b) 3 x $10^{14}/cm^2$, 1 keV P^+. Annealing conditions were 950°C for 10 sec. SIMS depth profiles of 1 x $10^{15}/cm^2$ B implanted at 0.5-, 1-, 2-, and 5 keV (c) as-implanted, and (d) after annealing at 1050°C for 10 sec. Copyright 1997 IEEE. Reprinted with permission from Ref. [13].

Ion Implantation
Shallow Implantation



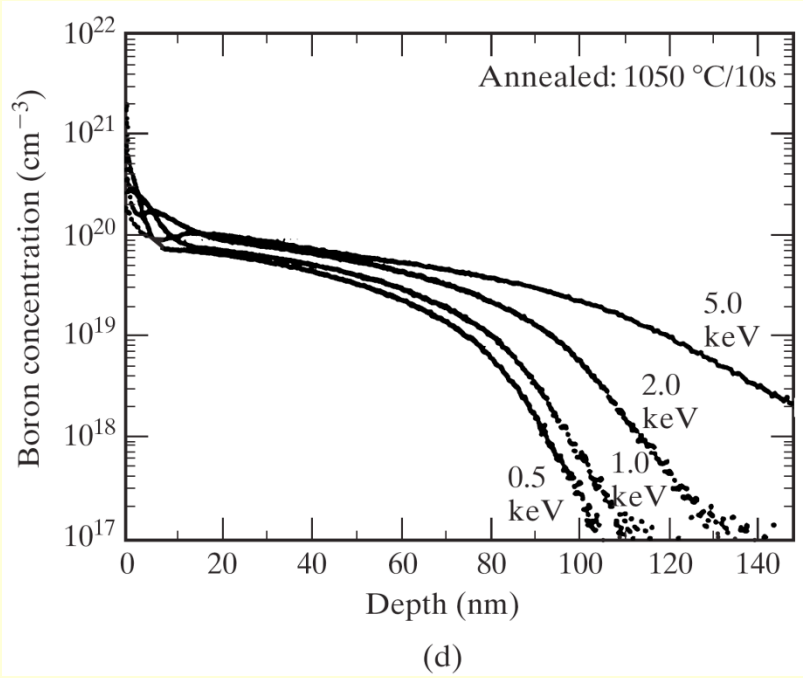
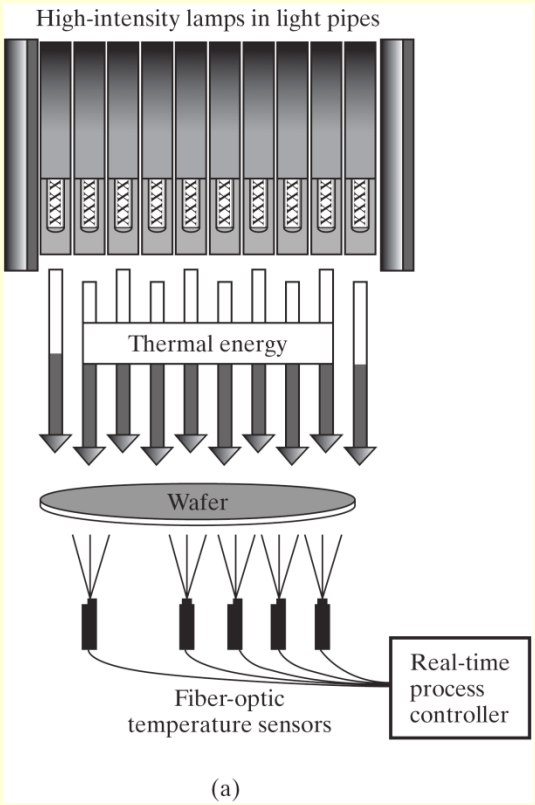


FIGURE 5.11

Examples of transient enhanced diffusion. SIMS data comparing as-implanted and annealed depth profiles from (a) 3 x 10^{14}/cm^2, 2 keV As$^+$, and (b) 3 x 10^{14}/cm^2, 1 keV P$^+$. Annealing conditions were 950°C for 10 sec. SIMS depth profiles of 1 x 10^{15}/cm^2 B implanted at 0.5-, 1-, 2-, and 5 keV (c) as-implanted, and (d) after annealing at 1050°C for 10 sec. Copyright 1997 IEEE. Reprinted with permission from Ref. [13].

Ion Implantation
Rapid Thermal Annealing



- Rapid Heating
- 950-1050^{o} C
- 50^{o} C/sec
- Very Low Dt

(b)

Figure 5.12
(a) Concept for a rapid thermal annealing (RTP) system. (b) Applied Materials 300 mm RTP System (Courtesy Applied Materials)

Ion Implantation References

[1] J. Lindhard, M. Scharff, and H. Schiott, "Range Concepts in Heavy Ion Ranges," *Mat.-Fys. Med. Dan. Vid. Selsk*, *33*, No. 14, 1963.

[2] J. F. Gibbons, W. S. Johnson, and S. W. Mylroie, *Projected Range in Semiconductors*, Second Edition, Dowden, Hutchinson, and Ross, New York, 1975.

[3] (a) L. Pauling and R. Hayward, *The Architecture of Molecules*, W. H. Freeman, San Francisco, 1964. (b) S. M. Sze, Ed., *Semiconductor Devices Physics and Technology*, McGraw-Hill, New York, 1985.

[4] S. Furukawa, H. Matsumura, and H. Ishiwara, "Lateral Distribution Theory of Implanted Ions," in S. Namba, Ed., *Ion Implantation in Semiconductors*, Japanese Society for the Promotion of Science, Kyoto, p. 73 (1972).

[5] G. Dearnaley, J. H. Freeman, G. A. Card, and M. A. Wilkins, "Implantation Profiles of ^{32}P Channeled into Silicon Crystals," *Canadian Journal of Physics, 46*, 587–595 (March 15, 1968).

[6] F. F. Morehead and B. L. Crowder, "A Model for the Formation of Amorphous Si by Ion Implantation," p. 25–30, in Eisen and Chadderton (see Source Listing 4).

[7] B. L. Crowder and F. F. Morehead, Jr., "Annealing Characteristics of *n*-type Dopants in Ion-Implanted Silicon," *Applied Physics Letters, 14*, 313–315 (May 15, 1969).

[8] W. K. Hofker, "Implantation of Boron in Silicon," *Philips Research Reports Supplements*, No. 8, 1975.

[9] J. F. Gibbons, "Ion-Implantation in Semiconductors—Part I: Range Distribution Theory and Experiment," *Proceedings of the IEEE, 56*, 295–319 (March, 1968).

[10] J. F. Gibbons, "Ion Implantation in Semiconductors—Part II: Damage Production and Annealing," *Proceedings of the IEEE, 60*, 1062–1096 (September, 1972).

[11] T. Hirao, G. Fuse, K. Inoue, S. Takayanagi, Y. Yaegashi, S. Ichikawa, and T. Izumi, "Electrical Properties of Si Implanted with As Through SiO_2 Films," *Journal of Applied Physics, 51*, 262–268 (January, 1980).

[12] K. Goto, J. Matsuo, Y. Tada, T. Tanaka, Y. Momiyama, T. Sugii, I. Yamada, "A High Performance 50 nm PMOSFET Using Decaborane ($B_{10}H_{14}$) Ion Implantation and 2-step Activation Annealing Process," *IEEE IEDM Digest*, pp. 471–474, December 1997.

[13] A. Agarwal, D. J. Eaglesham, H-J. Gossman, L. Pelaz, S. B. Herner, D. C. Jacobson, T. E. Haynes, Y. Erokhin and R. Simonton, "Boron-Enhanced-Diffusion of Boron: The Limiting Factor for Ultra Shallow Junctions, *IEEE IEDM Digest*, pp. 467–470, December 1997.

[14] A. D. Lilak, S. K. Earles, K. S. Jones, M. E. Law and M. D. Giles, "A Physics-based Modeling Approach for the Simulation of Anomalous Boron Diffusion and Clustering Behavior," *IEEE IEDM Digest*, pp. 493–496, December 1997.

[15] K. Suzuki, T. Miyashita and Y. Tada, "Damage Calibration Concept and Novel B Cluster Reaction Model for B Transient Enhanced Diffusion Over Thermal Process Range from 600 C (839 h) to 1,100 °C (5 s) with Various Ion Implantation Doses and Energies," *IEEE IEDM Digest*, pp. 501–504, December 1997.

[16] S. S. Yu, H. W. Kennel, M. D. Giles and P. A. Packan, "Simulation of Transient Enhanced Diffusion Using Computationally Efficient Models," *IEEE IEDM Digest*, pp. 509–512, December 1997.

SOURCE LISTING

[1] J. W. Mayer, L. Eriksson, and J. A. Davies, *Ion-Implantation in Semiconductors*, Academic Press, New York, 1970.

[2] G. Dearnaley, J. H. Freeman, R. S. Nelson, and J. Stephen, *Ion-Implantation*, North-Holland, New York, 1973.

[3] G. Carter and W. A. Grant, *Ion-Implantation of Semiconductors*, John Wiley & Sons, New York, 1976.

[4] F. Eisen and L. Chadderton, Eds., *Ion Implantation in Semiconductors*, First International Conference (Thousand Oaks, CA), Gordon and Breach, New York, 1970.

[5] I. Ruge and J. Graul, Eds., *Ion Implantation in Semiconductors*, Second International Conference (Garmisch-Partenkirchen, West Germany), Springer-Verlag, Berlin, 1972.

[6] B. L. Crowder, Ed., *Ion Implantation in Semiconductors*, Third International Conference (Yorktown Heights, NY), Plenum, New York, 1973.

[7] S. Namba, Ed., *Ion Implantation in Semiconductors*, Fourth International Conference (Osaka, Japan), Plenum, New York, 1975.

[8] F. Chernow, J. Borders, and D. Bruce, Eds., *Ion Implantation in Semiconductors*, Fifth International Conference (Boulder, CO), Plenum, New York, 1976.

Copyright Notice

© 2002 Pearson Education, Inc., Upper Saddle River, NJ. All rights reserved. This material is protected under all copyright laws as they currently exist. No portion of this material may be reproduced, in any form or by any means, without permission in writing from the publisher.

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

End of Chapter 5

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.