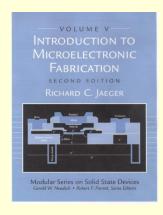
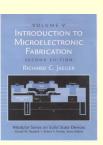
## Introduction to Microelectronic Fabrication

Chapter 3
Thermal Oxidation of Silicon

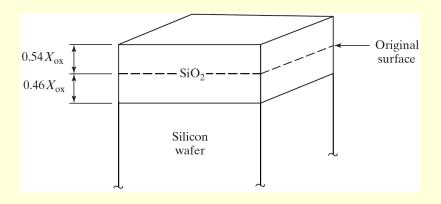




### Thermal Oxidation of Silicon

Silicon Dioxide

High quality electrical insulator Diffusion/implantation barrier Passivates silicon surface



**Dry Oxidation** 

$$Si + O_2 \rightarrow SiO_2$$

Wet Oxidation

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

Growth Occurs 54% above and 46% below original surface as silicon is consumed

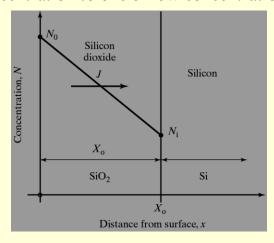
### Thermal Oxidation Fick's First Law of Diffusion

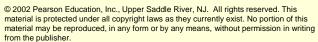


Particle flux J is proportional to the negative of the gradient of the particle concentration

$$J = -D \frac{\partial N}{\partial x}$$
 D = diffusion coefficient

Particles move from a region of high concentration to one of low concentration





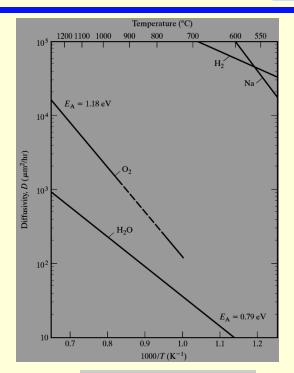


FIGURE 3.1

Diffusivities of hydrogen, oxygen, sodium, and water vapor in silicon glass. Copyright John Wiley & Sons, Inc. Reprinted with permission from Ref. [4].

### Thermal Oxidation Fick's First Law of Diffusion



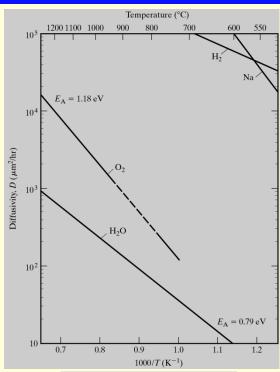
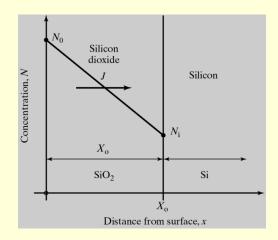


FIGURE 3.1

Diffusivities of hydrogen, oxygen, sodium, and water vapor in silicon glass. Copyright John Wiley & Sons, Inc. Reprinted with permission from Ref. [4].



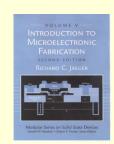
$$D = D_O \exp\left(-\frac{E_A}{kT}\right)$$
 Arrhenius Relationship

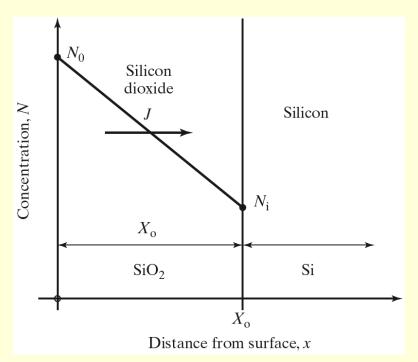
 $E_A = activation energy$ 

 $k = Boltzmann's constant = 1.38 x 10^{-23} J/K$ 

T = absolute temperature

## Thermal Oxidation Oxidation Theory





$$J = -D \frac{\partial N(x,t)}{\partial x} = -D \frac{(N_i - N_0)}{X_O}$$
$$J(X_o) = k_s N_i$$

$$t = \frac{X_o^2}{B} + \frac{X_o}{\left(B/A\right)} - \tau \qquad \tau = \frac{X_i^2}{B} + \frac{X_i}{\left(B/A\right)}$$

$$A = \frac{2D}{k_s} \qquad B = \frac{2DN_0}{M}$$

$$X_o(t) = 0.5A \left[ \left\{ 1 + 4 \frac{B}{A^2} (t + \tau) \right\}^{0.5} - 1 \right]$$

Oxide growth occurs at X<sub>o</sub>

 $X_o$  = final oxide thickness

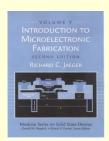
 $X_i$  = initial oxide thickness

D = diffusion coefficient

N =concentration of oxygen

 $\tau$  = time required to grow initial oxide k<sub>s</sub> = rate constant at  $S_i - S_i O_2$  interface

## Oxidation Theory Parabolic Regime



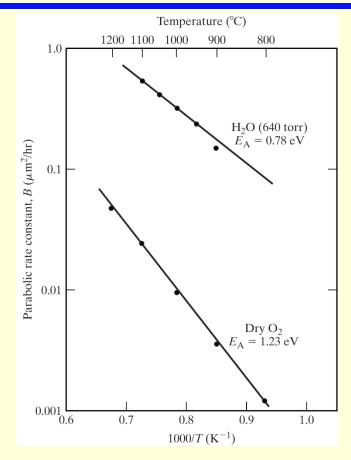
For Long Times 
$$-(t+\tau) >> \frac{A^2}{4B}$$

$$X_o(t) = \sqrt{Bt}$$

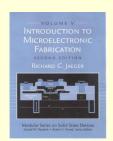
B = parabolic rate constant

#### FIGURE 3.4

Dependence of the parabolic rate constant B on temperature for the thermal oxidation of silicon in pyrogenic H<sub>2</sub>O (640 torr) or dry O<sub>2</sub>. Reprinted by permission of the publisher, The Electrochemical Society, Inc., from Ref. [10].



### Oxidation Theory Linear Regime



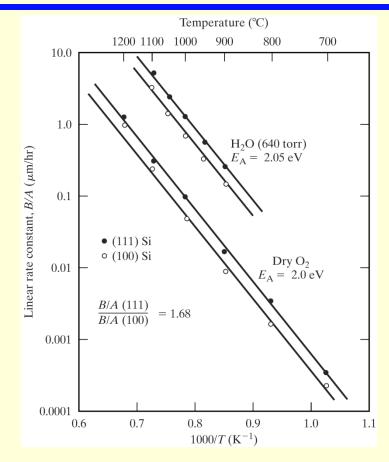
For Short Times 
$$-(t+\tau) << \frac{A^2}{4B}$$

$$X_o(t) \cong \left(\frac{B}{A}\right)(t+\tau)$$

$$\left(\frac{B}{A}\right)$$
 = linear rate constant

#### FIGURE 3.5

Dependence of the linear rate constant B/A on temperature for the thermal oxidation of silicon in pyrogenic  $H_2O$  (640 torr) or dry  $O_2$ . Reprinted by permission of the publisher, The Electrochemical Society, Inc., from Ref. [10].



## Rate Constants Wet and Dry Oxidation

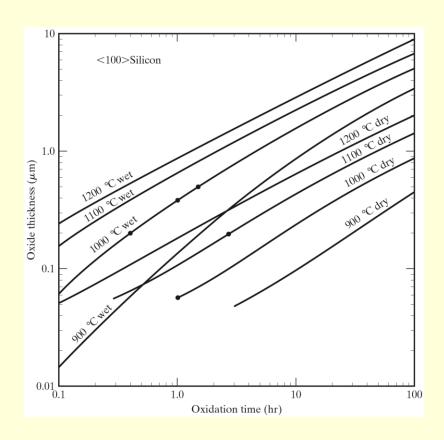


	Wet $O_2(X_i = 0 \text{ nm})$		$Dry O_2(X_i = 25 nm)$		
	$\mathbf{D}_0$	$E_{A}$	$\mathbf{D}_0$	$E_A$	
<100> Silicon					
Linear (B/A)	$9.70 \times 10^7 \mu \text{m/hr}$	2.05 eV	$3.71 \times 10^6 \mu$ m/hr	2.00 eV	
Parabolic (B)	386µm²}/hr	$0.78\mathrm{eV}$	$772\mu \mathrm{m}^2/\mathrm{hr}$	1.23 eV	
<111> Silicon					
Linear (B/A)	$1.63 \times 10^{8} \mu \text{m/hr}$	2.05 eV	$6.23\mu 10^6 \mu m/hr$	2.00 eV	
Parabolic (B)	$386\mu \text{m}^2/\text{hr}$	$0.78\mathrm{eV}$	$772\mu \text{m}^2/\text{hr}$	1.23 eV	

- Wet oxidation is much more rapid than dry oxidation
- Note that dry oxidation appears to always have some initial oxide present
- Dry oxidation (slow) produces higher quality oxide than wet oxidation

## Thermal Oxidation Oxidation on <100> Silicon



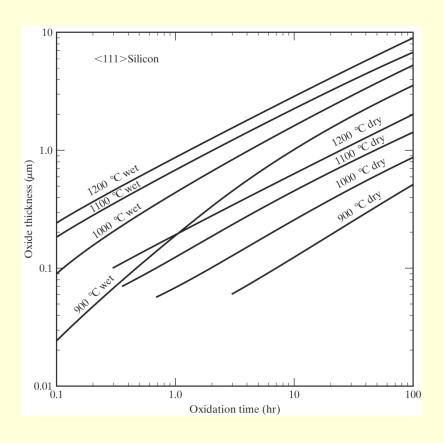


#### FIGURE 3.6

Wet and dry silicon dioxide growth for <100> silicon calculated using the data from Table 3.1. (The dots represent data used in examples.)

## Thermal Oxidation Oxidation on <111> Silicon





#### FIGURE 3.7

Wet and dry silicon dioxide growth for <111> silicon calculated using the data from Table 3.1.

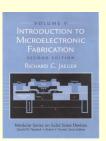


### Thermal Oxidation Example

#### Example 3.2

A <100> wafer has a 2000-Å oxide on its surface.

- (a) How long did it take to grow this oxide at 1100 °C in dry oxygen?
- **(b)** The wafer is put back in the furnace in wet oxygen at 1000 °C. How long will it take to grow an additional 3000 Å of oxide? Solve this problem graphically using Figs. 3.6 and 3.7 as appropriate.
- (c) Repeat part (b) using the oxidation theory presented in Eqs. (3.3) through (3.12). **Solution:** (a) According to Fig. 3.6, it would take 2.8 hr to grow a 0.2- $\mu$ m oxide in dry oxygen at 1100 °C.
- (b) We can solve part (b) graphically using Fig. 3.6. The total oxide at the end of the oxidation would be 0.5  $\mu$ m. If there were no oxide on the surface, it would take 1.5 hr to grow 0.5  $\mu$ m. However, there is already a 0.2 $\mu$ m oxide on the surface, and the wafer "thinks" that it has already been in the furnace for 0.4 hr. The time required to grow the additional 0.3  $\mu$ m of oxide is the difference in these two times:  $\Delta t = (1.5 0.4) \text{ hr} = 1.1 \text{ hr}$ .
- (c) From Table 3.1,  $B = 3.86 \times 10^{-2} \exp(-0.78/kT) \, \mu m^{-2}/hr$  and  $(B/A) = 0.97 \times 10^{8} \exp(-2.05/kT) \, \mu m/hr$ . Using  $T = 1,273 \, K$  and  $k = 8.617 \times 10^{-5} \, eV/Kg$ ,  $B = 0.314 \, \mu m^{2} \times hr$  and  $(B/A) = 0.738 \, \mu m/hr$ . Using these values and an initial oxide thickness of 0.2m yields a value of 0.398 hr for the effective initial oxidation time  $\tau$ . Using  $\tau$  and a final oxide thickness of 0.5  $\mu$ m yields an oxidation time of 1.08 hr. Note that both the values of t and  $\tau$  are close to those found in part (b). Of course, the graphical results depend on our ability to interpolate logarithmic scales!



### Thermal Oxidation Example

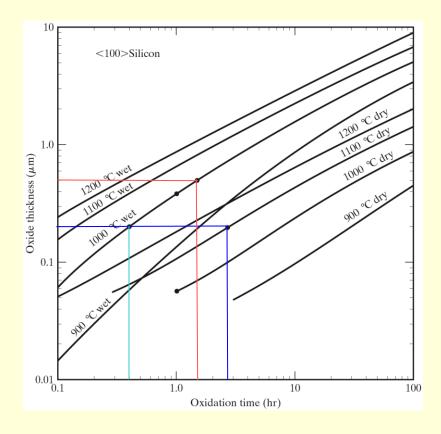
A <100> silicon wafer has a 2000-Å oxide on its surface

(a) How long did it take to grow this oxide at 1100°C in dry oxygen?

(b) The wafer is put back in the furnace in wet oxygen at 1000° C. How long will it take to grow an additional 3000 Å of oxide?

## Thermal Oxidation Example Graphical Solution





- (a) According to Fig. 3.6, it would take2.8 hr to grow 0.2 μm oxide in dry oxygen at 1100° C.
- (b) The total oxide thickness at the end of the oxidation would be  $0.5 \mu m$  which would require 1.5 hr to grow if there was no oxide on the surface to begin with. However, the wafer "thinks" it has already been in the furnace 0.4 hr. Thus the additional time needed to grow the  $0.3 \mu m$  oxide is 1.5-0.4 = 1.1 hr.

## Thermal Oxidation Example Mathematical Solution



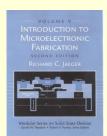
(a) From Table 3.1,

$$B = 7.72x10^{2} \exp\left(\frac{-1.23}{kT}\right) \frac{\mu m^{2}}{hr} \qquad \frac{B}{A} = 3.71x10^{6} \exp\left(\frac{-2.00}{kT}\right) \frac{\mu m}{hr} \qquad X_{i} = 25nm$$
For T = 1273 K, B = 0.0236  $\frac{\mu m^{2}}{hr}$  and  $\frac{B}{A} = 0.169 \frac{\mu m}{hr}$ 

$$\tau = \frac{\left(0.025 \mu m\right)^2}{0.0236 \frac{\mu m^2}{hr}} + \frac{0.025 \mu m}{0.169 \frac{\mu m}{hr}} = 0.174 \ hr$$

$$t = \frac{\left(0.2\mu m\right)^2}{0.0236\frac{\mu m^2}{hr}} + \frac{0.2\mu m}{0.169\frac{\mu m}{hr}} - 0.174hr = 2.70 \ hr$$

## Thermal Oxidation Example Mathematical Solution



(b) From Table 3.1,

(b) From Table 5.1,  

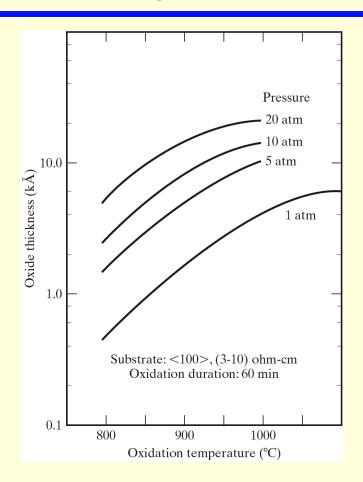
$$B = 3.86x10^{2} \exp\left(\frac{-0.78}{kT}\right) \frac{\mu m^{2}}{hr} \qquad \frac{B}{A} = 9.70x10^{7} \exp\left(\frac{-2.05}{kT}\right) \frac{\mu m}{hr} \qquad X_{i} = 0$$
For T = 1273 K, B = 0.314  $\frac{\mu m^{2}}{hr}$  and  $\frac{B}{A} = 0.742 \frac{\mu m}{hr}$ 

$$\tau = \frac{\left(0.2\mu m\right)^{2}}{0.314 \frac{\mu m^{2}}{hr}} + \frac{0.2\mu m}{0.742 \frac{\mu m}{hr}} = 0.398 \ hr$$

$$t = \frac{\left(0.5\mu m\right)^{2}}{0.314 \frac{\mu m^{2}}{hr}} + \frac{0.5\mu m}{0.742 \frac{\mu m}{hr}} - 0.398 hr = 1.07 \ hr$$

# Thermal Oxidation Wet High Pressure Oxidation

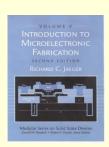


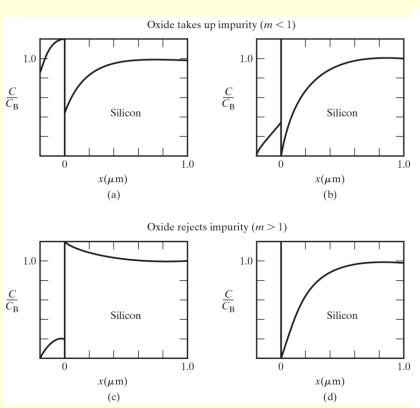


#### FIGURE 3.8

Wet oxide growth at increased pressures. Reprinted with permission of Solid State Technology, published by Technical Publishing, a company of Dun and Bradstreet, from Ref. [12].

# Thermal Oxidation Impurity Redistribution



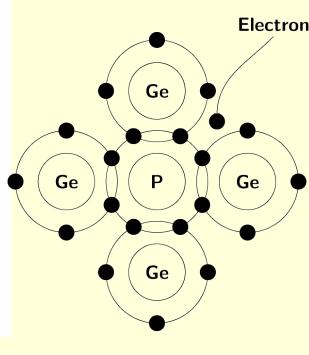


#### FIGURE 3.9

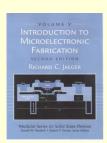
The effects of oxidation on impurity profiles.

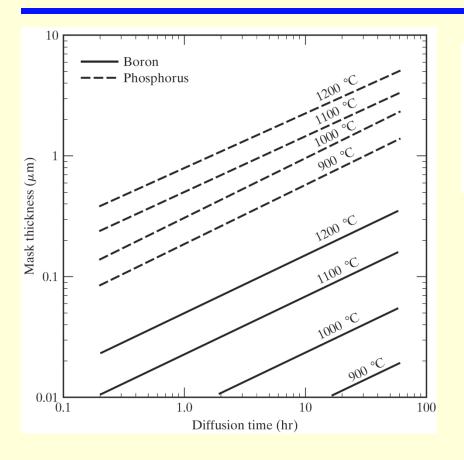
(a) Slow diffusion in oxide (boron); (b) fast diffusion in oxide (boron with hydrogen ambient); (c) slow diffusion in oxide (phosphorus); (d) fast diffusion in oxide (gallium).  $C_B$  is the bulk concentration in the silicon. Copyright John Wiley & Sons, Inc. Reprinted with permission from Ref. [5].

$$m = \frac{dopant\ concentration\ in\ Si}{dopant\ concentration\ in\ SiO_2}$$



# Thermal Oxidation Masking Properties of SiO<sub>2</sub>





#### **FIGURE 3.10**

Thickness of silicon dioxide needed to mask boron and phosphorus diffusions as a function of diffusion time and temperature.

- Required oxide thickness depends upon dopant species and temperature
- Hydrogen greatly enhances diffusion of boron - wet oxidation release hydrogen

# Thermal Oxidation Oxide Quality



- Dry oxidation (slow) produces higher quality oxide than wet oxidation
- Oxidations often consist of sequence of dry-wet-dry oxidation cycles -Most of oxide is grown during wet phase
- Dry phase yields higher density oxide with improved breakdown voltage (5-10 MV/cm)
- Dry oxidation usually used to grow gate oxides
- Nitrogen being added to form oxynitrides for very thin gate oxides

# Thermal Oxidation Oxidation Systems



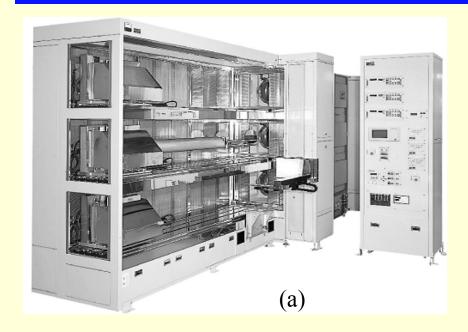


Figure 3.11 Furnaces used for oxidation and diffusion (a) A three-tube horizontal furnace with multizone temperature control

(b) Vertical furnace (Courtesy of Crystec, Inc.)



(b)

### Local Oxidation of Silicon (LOCOS)



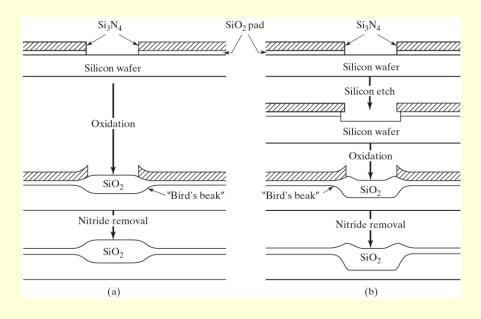


FIGURE 3.12

Cross section depicting process sequence for local oxidation of silicon (LOCOS): (a) semirecessed and (b) fully recessed structures.

- Isolation technology in MOS processes
- Provides isolation between nearby devices
- Fully recessed process attempts to minimize bird's beak

# Thermal Oxidation Deep Trench Isolation



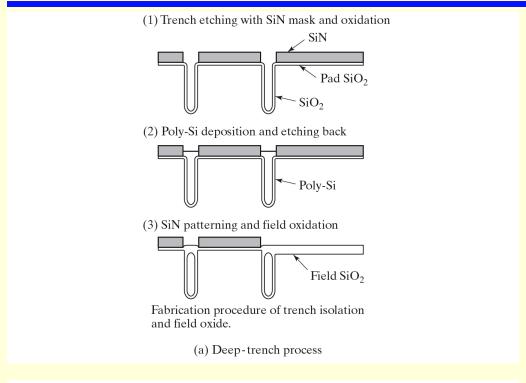


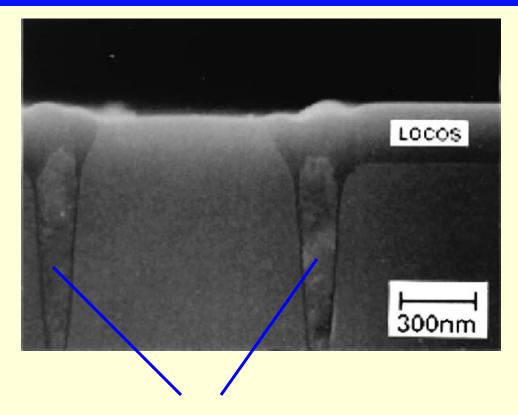
FIGURE 3.13

Trench isolation structures. (a) Deep trench isolation - Copyright 1996 IEEE. Reprinted with permission from Ref. [18]. (b) Shallow trench isolation - Copyright 1998 IEEE. Reprinted with permission from Ref. [20].

- Often used in dynamic memory chips (DRAMS)
- Deep trenches used in high performance bipolar processes

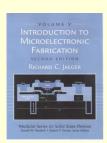
# Thermal Oxidation Example of Deep Trenches

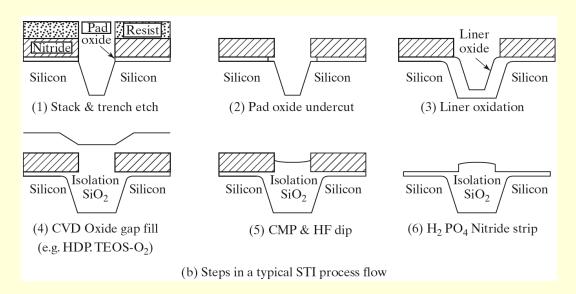




Filled Trenches

## Thermal Oxidation Shallow Trench Isolation





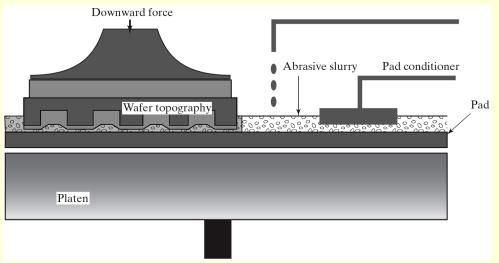
Used for isolation between devices and to minimize device capacitance

#### FIGURE 3.13

Trench isolation structures. (a) Deep trench isolation - Copyright 1996 IEEE. Reprinted with permission from Ref. [18]. (b) Shallow trench isolation - Copyright 1998 IEEE. Reprinted with permission from Ref. [20].

# Chemical Mechanical Polishing (CMP)

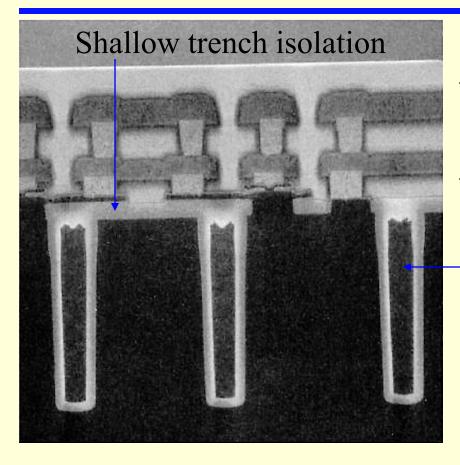




- Mechanical polishing is widely used to achieve highly planar surfaces
- Used in multilevel metalization systems including both aluminum and copper

# Thermal Oxidation Trench Isolation Example





CMP planarization

Deep trench isolation

Figure 3.14 Microphotograph of actual deep and shallow trench isolation applied to SiGE HBT technology. Copyright 1998 IEEE. Reprinted with permission from Ref. [31].

# Multilevel Metallization Using CMP



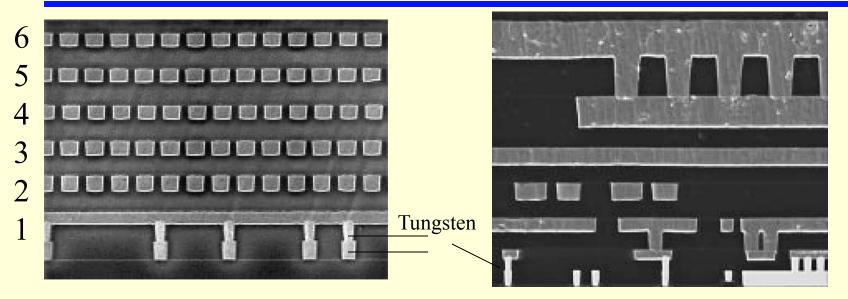


Figure 3.16 Multilevel metallization fabricated with chemical mechanical polishing (a) SEM of 6-level thin-wire copper. First-level copper is connected with tungsten studs to tungsten local interconnect. (b) SEM of 6-level copper with low RC metallization on levels 5 and 6. Copyright 1997 IEEE. Reprinted with permission from Ref. [24].

### Oxide Thickness Determination

 $\begin{tabular}{ll} TABLE 3.2 & Color Chart for Thermally Grown SiO_2 Films Observed Perpendicularly Under Daylight Fluorescent Lighting. Copyright 1964 by International Business Machines Corporation; reprinted with permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Daylight Fluorescent Properties of the permission of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \begin{tabular}{ll} Fluorescent Properties of the permission from Ref. [11]. \\ \be$ 

Film Thickness		Film Thickness	
(µm)	Color and Comments	(µm)	Color and Comments
0.05	Tan	0.58	Light orange or yellow to pink
0.07	Brown	0.60	Carnation pink
0.10	Dark violet to red violet	0.63	Violet red
0.12	Royal blue	0.68	"Bluish" (not blue but borderline
0.15	Light blue to metallic blue		between violet and blue green; appears
0.17	Metallic to very light		more like a mixture between violet
	yellow green		red and blue green and looks grayish)
0.20	Light gold or yellow;	0.72	Blue green to green (quite broad)
	slightly metallic	0.77	"Yellowish"
0.22	Gold with slight	0.80	Orange (rather broad for orange)
	yellow orange	0.82	Salmon
0.25	Orange to melon	0.85	Dull, light red violet
0.27	Red violet	0.86	Violet
0.30	Blue to violet blue	0.87	Blue violet
0.31	Blue	0.89	Blue
0.32	Blue to blue green	0.92	Blue green
0.34	Light green	0.95	Dull yellow green
0.35	Green to yellow green	0.97	Yellow to "yellowish"
0.36	Yellow green	0.99	Orange
0.37	Green yellow	1.00	Carnation pink
0.39	Yellow	1.02	Violet red
0.41	Light orange	1.05	Red violet
0.42	Carnation pink	1.06	Violet
0.44	Violet red	1.07	Blue violet
0.46	Red violet	1.10	Green
0.47	Violet	1.11	Yellow green
0.48	Blue violet	1.12	Green
0.49	Blue	1.18	Violet
0.50	Blue green	1.19	Red violet
0.52	Green (broad)	1.21	Violet red
0.44	Violet red	1.24	Carnation pink to salmon
0.46	Red violet	1.25	Orange
0.47	Violet	1.28	"Yellowish"
0.48	Blue violet	1.32	Sky blue to green blue
0.49	Blue	1.40	Orange
0.50	Blue green	1.45	Violet
0.52	Green (broad)	1.46	Blue violet
0.54	Yellow green	1.50	Blue
0.56	Green yellow	1.54	Dull yellow green
0.57	Yellow to "yellowish" (not yellow but		
	is in the position where yellow is to be		
	expected; at times appears to be light		
	creamy gray or metallic)		



#### Oxide Color Chart

Oxide thickness for constructive interference

$$2X_o = \frac{k\lambda}{n}$$

 $n = index of refraction (1.46 for SiO_2)$ 

$$k \in [1, 2, 3, ...]$$

Ellipsometer - direct measurement

### Oxide Thickness Determination

#### SiO<sub>2</sub> Thickness Color Chart

EOO	ss (Å) Color of Film (those shown are only indicative			
500 700	tan			
1000	brown			
1200	dark violet to red violet roval blue			
1500	light blue to metallic blue			
1700	metallic to very light yellow-green			
2000	light gold or yellow - slightly metallic			
2200	gold with slight yellow-orange			
2500	orange to melon			
2700	red-violet			
3000	blue to violet-blue			
3100	blue			
3200	blue to blue-green			
3400	light green			
3500	green to yellow-green			
3600	vellow-green			
3700	green-vellow			
3900	vellow			
4100	light orange			
4200	carnation pink			
4400	violet-red			
4600	red-violet			
4700	violet			
4800	blue-violet			
4900	blue			
5000	blue-green			
5200	green			
5400	yellow-green			
5600	green-yellow			
	yellow to "yellowish" (at times appears light			
5700	gray or metallic)			
5800	light orange or yellow to pink			
6000	carnation pink			
6300	violet-red			
	"bluish" (appears between violet-red and			
6800	blue-green - overall looks grayish			
7200	blue-green to green			
7700	"yellowish"			
8000	orange			
8200	salmon			
8500	dull light red-violet			
8600	violet			
8700	blue-violet			
8900	blue			
9200	blue-green			
9500	dull yellow-green			
9700	yellow to "yellowish"			



#### Oxide Color Chart

Oxide thickness for constructive interference

$$2X_o = \frac{k\lambda}{n}$$

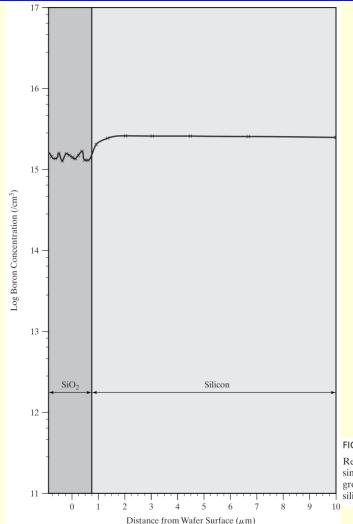
 $n = index of refraction (1.46 for SiO_2)$ 

$$k \in [1, 2, 3, ...]$$

• Ellipsometer - direct measurement

### Process Simulation SUPREM Oxidation Example





#### **SUPREM**

Stanford University Process
Engineering Modeling Program
[25-27]

#### http://www-tcad.stanford.edu/

```
TABLE 3.3 SUPREM-IV Simulation Example

$ Multistep Oxidation

$ Use Automatic Grid Generation and Adaptive Grid

INITIALIZE <100> BORON = 5 RESISTIV

DIFFUSION TEMP=950 TIME=30 F.N2 = 5

DIFFUSION TEMP=950 TIME=30 T.FINAL = 1100 F.O2 = 5

DIFFUSION TEMP=1100 TIME=300 STEAM

DIFFUSION TEMP=1100 TIME=60 F.O2 = 5

DIFFUSION TEMP=1100 TIME=60 T.FINAL = 800 F.N2 = 5

$ Print layer information

....

$ Plot results
....
```

FIGURE 3.17
Results of SUPREM simulation of oxide growth on boron doped silicon wafers.

## Thermal Oxidation References



- [1] W. R. Runyon and K. E. Bean, Semiconductor Integrated Circuit Processing Technology, Addison Wesley, Reading, MA, 1990.
- [2] S. A. Campbell, *The Science and Engineering of Microelectronic Fabrication*, Oxford University Press, 1996.
- [3] S. M. Sze, VLSI Technology, McGraw-Hill, New York, 1983.
- [4] S. K. Ghandhi, VLSI Fabrication Principles, John Wiley & Sons, New York, 1983.
- [5] R. A. Colclaser, Microelectronics—Processing and Device Design, John Wiley & Sons, New York, 1980.
- [6] W. R. Runyan, Semiconductor Measurements and Instrumentation, McGraw-Hill, New York, 1975.
- [7] S. K. Ghandhi, The Theory and Practice of Microelectronics, John Wiley & Sons, New York, 1968.
- [8] B. E. Deal and A. S. Grove, "General Relationship for the Thermal Oxidation of Silicon," *Journal of Applied Physics*, 36, 3770–3778 (December, 1965).
- B. E. Deal, "Thermal Oxidation Kinetics of Silicon in Pyrogenic H<sub>2</sub>O and 5% HCL/H<sub>2</sub>O Mixtures," *Journal of the Electrochemical Society*, 125, 576–579 (April, 1978).
- [10] B. E. Deal, "The Oxidation of Silicon in Dry Oxygen, Wet Oxygen and Steam," *Journal of the Electrochemical Society*, 110, 527–533 (June, 1963).
- [11] W. A. Pliskin and E. E. Conrad, "Nondestructive Determination of Thickness and Refractive Index of Transparent Films," *IBM Journal of Research and Development*, 8, 43–51 (January, 1964).
- [12] S. C. Su, "Low Temperature Silicon Processing Techniques for VLSIC Fabrication," *Solid-State Technology*, 24, 72–82 (March, 1981).
- [13] A. S. Grove, O. Leistiko, and C. T. Sah, "Redistribution of Acceptor and Donor Impurities During Thermal Oxidation of Silicon," *Journal of Applied Physics*, 35, 2695–2701 (September, 1964).
- [14] A. S. Grove, Physics and Technology of Semiconductor Devices, John Wiley & Sons, New York, 1967.
- [15] E. H. Nicollian and J. R. Brews, MOS Physics and Technology, John Wiley & Sons, New York, 1982.
- [16] M. Ghezzo and D. M. Brown, "Diffusivity Summary of B, Ga, P, As and Sb in SiO<sub>2</sub>," *Journal of the Electrochemical Society*, 120, 146–148 (January, 1973).

- [17] E. Passaglia, R. R. Stromberg, and J. Kruger, Eds., *Ellipsometry in the Measurement of Surfaces and Thin Films*, National Bureau of Standards, Miscellaneous Publication #256, 1964.
- [18] H. Kotaki et al., "Novel Bulk Dynamic Threshold Voltage MOSFET (B-DTMOS) with Advanced Isolation (SITOS) and Gate to Shallow-Well Contact (SSS-C) Processes for Ultra Low Power Dual Gate CMOS," IEEE IEDM Technical Digest, pp. 459–462, December 1996.
- [19] K. P. Muller, B. Flietner, C. L. Hwang, R. L. Kleinhenz, T. Nakao, R. Ranade, Y. Tsunashima, and T. Mii, "Trench Storage Node Technology for Gigabit DRAM Generations," *IEEE IEDM Technical Digest*, pp. 507–510, December 1996.
- [20] M. Nandakumar, A. Chatterjee, S. Sridhar, K. Joyner, M. Rodder, and I-C. Chen, "Shallow Trench Isolation for Advanced ULSI CMOS Technologies," *IEEE IEDM Technical Digest*, pp. 133–136, December 1998.
- [21] J. M. Steigerwald et al., "Pattern Geometry in Chemical-Mechanical Polishing of Inlaid Copper Structures," *Journal of the Electrochemical Society*, 141, no. 10: 2842–2848, Oct. 1994.
- [22] B. Stine et al., "Rapid Characterization and Modeling of Pattern-Dependent Variation in Chemical-Mechanical Polishing," *IEEE Trans. Semiconductor Manufacturing*, 11, no. 1, February 1998.
- [23] H. Nojo, M. Kodera, and R. Nakata, "Slurry Engineering for Self-Stopping Dishing Free SiO<sub>2</sub>-CMP," *IEEE IEDM Technical Digest*, pp. 349–352, December 1996.
- [24] D. Edelstein et al., "Full Copper Wiring in a Sub-0.25µm CMOS ULSI Technology," *IEEE IEDM Technical Digest*, pp. 773–776, December 1997.
- [25] D. A. Antoniadis and R. W. Dutton, "Models for Computer Simulation of Complete IC Fabrication Processes," *IEEE Journal of Solid-State Circuits*, SC-14, pp. 412–422, April 1979.
- [26] C. P. Ho, J. D. Plummer, S. E. Hansen, and R. W. Dutton, "VLSI Process Modeling—SUPREM III," *IEEE Trans. Electron Devices*, ED-30, pp. 1438–1453, November 1983.
- [27] D. Chin, M. Kump, H.G. Lee, and R. W. Dutton, "Process Design Using Coupled 2D Process and Device Simulators," *IEEE IEDM Technical Digest*, pp. 223–226, December 1986.
- [28] C. D. Maldanado, F. Z. Custode, S. A. Louie, and R. K. Pancholy, "Two-Dimensional Simulation of a 2µm CMOS Process Using ROMANS II," *IEEE Trans. Electron Devices*, ED-30, pp. 1462–1469, November 1983.
- [29] M. E. Law, C. S. Rafferty, and R. W. Dutton, "New n-well Fabrication Techniques Based upon 2D Process Simulation," *IEEE IEDM Technical Digest*, pp. 518–521, December 1986.
- [30] R. W. Dutton, "Modeling and Simulation for VLSI," *IEEE IEDM Technical Digest*, pp. 2–7, December 1986.

### End of Chapter 3