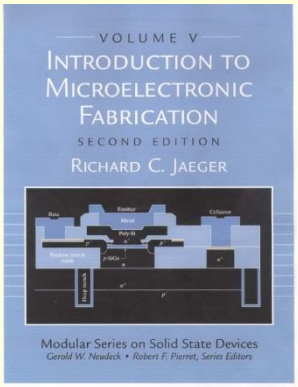
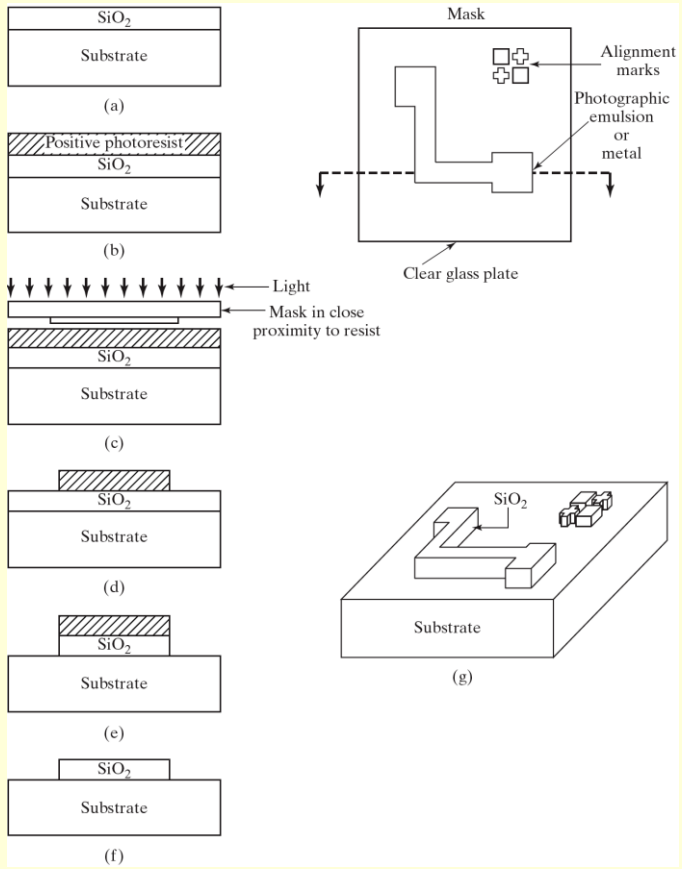
Introduction to Microelectronic Fabrication

Chapter 2
Photolithography



Photolithographic Process



(a) Substrate covered with silicon dioxide barrier layer

(b) Positive photoresist applied to wafer surface

(c) Mask in close proximity to surface

(d) Substrate following resist exposure and development

(e) Substrate after etching of oxide layer

(f) Oxide barrier on surface after resist removal

(g) View of substrate with silicon dioxide pattern on the surface

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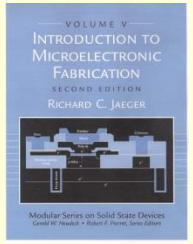
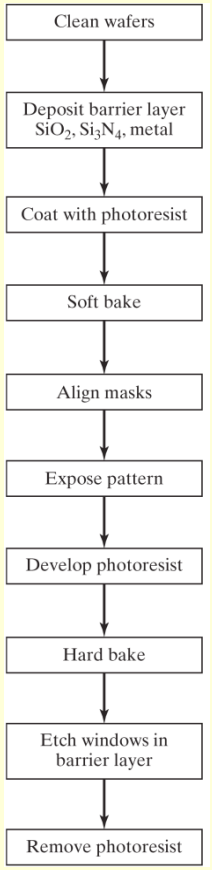
Photolithographic Process





- Each mask step requires many individual process steps
- Number of masks is a common measure of overall process complexity

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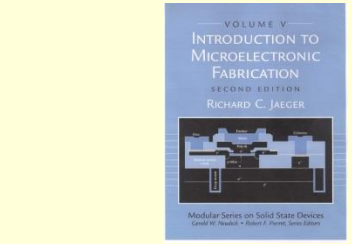
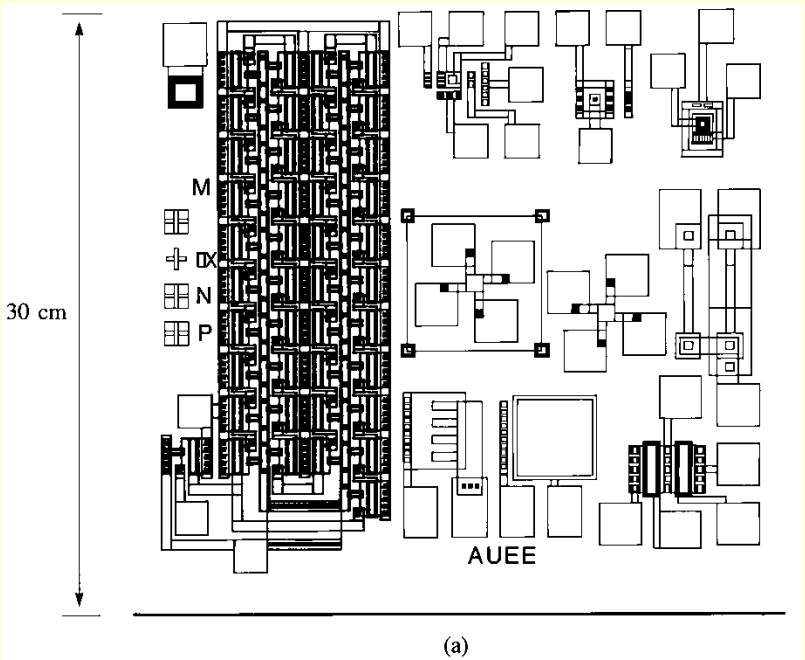
Photomasks
CAD Layout





- Composite drawing of the masks for a simple integrated circuit using a four-mask process
- Drawn with computer layout system
- Complex state-of-the-art CMOS processes may use 25 masks or more

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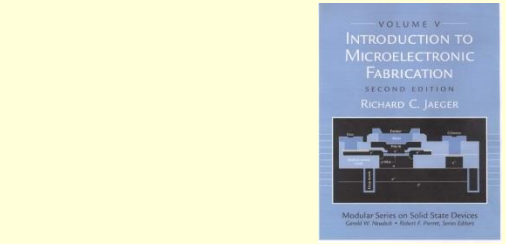
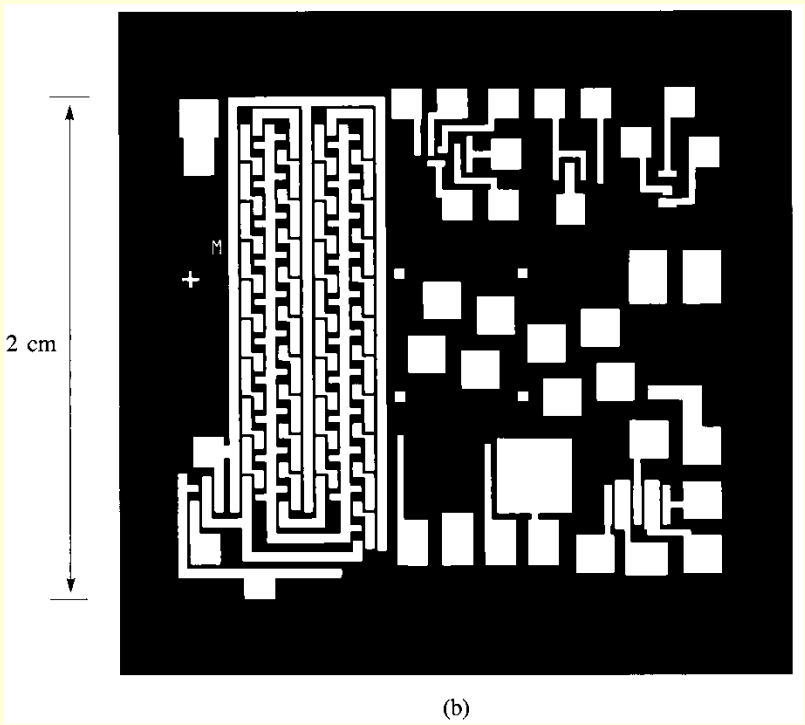
Photo Masks
10X Reticle





- Example of 10X reticle for the metal mask - this particular mask is ten times final size (10 μm minimum feature size - huge!)
- Used in step-and-repeat operation
- One mask for each lithography level in process

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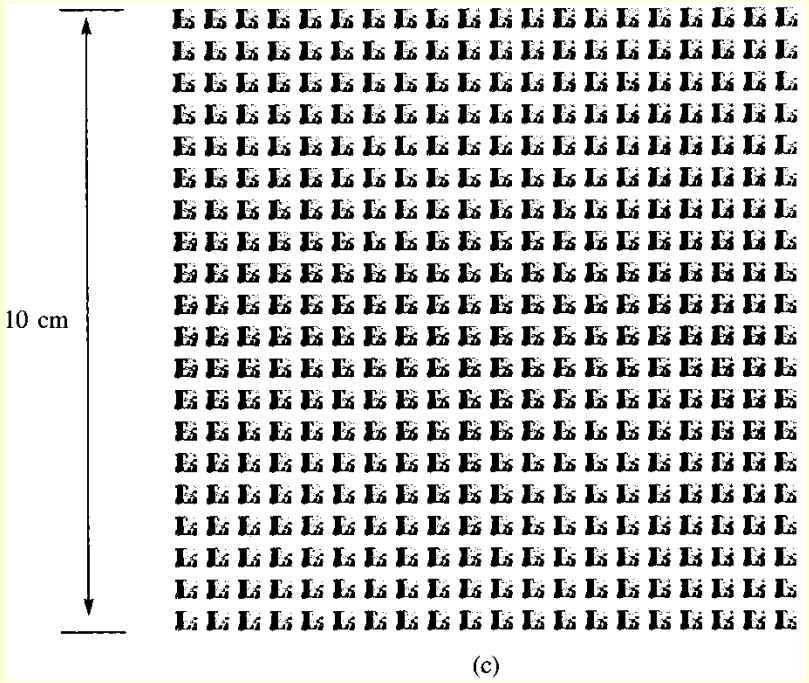
Photomasks
Final Mask



- Mask after reduction and "step-and-repeat" operation
- Final size emulsion mask with 400 copies of the metal level for the integrated circuit

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ITRS Lithography Projections

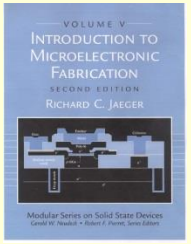

Table 2.5 -- ITRS Lithography Projections

Year	2001	2003	2005	2008	2011	2014
Dense Line Half-Pitch (nm)	150	120	100	70	50	35
Worst Case Alignment Tolerance Mean + 3 σ (nm)	52	42	35	25	20	15
Minimum Feature Size F (nm) Microprocessor Gate Width	100	80	65	45	30	20
Critical Dimension Control (nm) Mean + 3 σ - Post Etching	9	8	6	4	3	2
Equivalent Oxide Thickness (nm)	1.5 - 1.9	1.5 - 1.9	1.0 - 1.5	0.8 - 1.2	0.6 - 0.8	0.5 - 0.6
Lithography Technology Options	248 nm DUV	248 nm + PSM 193 nm DUV	193 nm + PSM 157 nm E-beam projection Proximity x-ray Ion Projection	157 nm +PSM E-beam projection E-beam direct write EUV Ion Projection Proximity x-ray	EUV E-beam projection E-beam direct write Ion Projection	EUV E-beam projection E-beam direct write Ion Projection Innovation

DUV - deep ultraviolet; EUV - extreme ultraviolet; PSM - phase shift mask;

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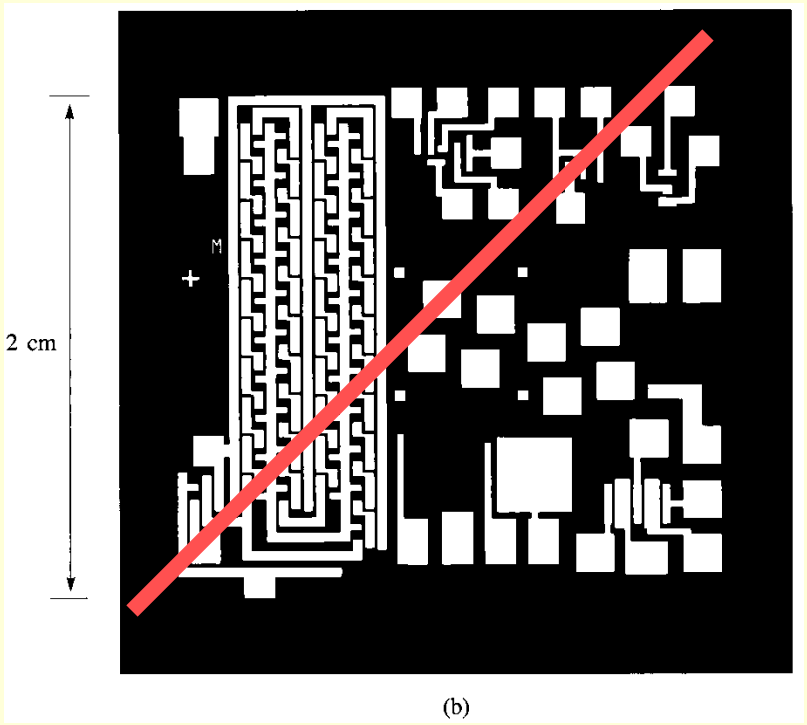
Contamination



- Human hair at the same scale as the integrated circuit with 10 μm feature size
- Today's feature size 100 nm - 100 times smaller!

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Clean Room Specifications

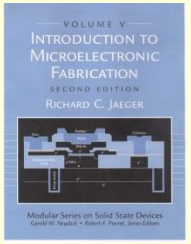

Table 2.1 Clean Room Ratings by Class of Filtration

Class	Number of 0.5μm particles per ft^3 (m^3)	Number of 5μm particles per ft^3 (m^3)
10,000	10000 (350,000)	65 (23,000)
1,000	1000 (35,000)	6.5 (2,300)
100	100 (3,500)	0.65 (230)
10	10 (350)	0.065 (23)
1	1 (35)*	0.0065 (2.3)

*It is very difficult to measure particulate counts below 1 0/ft^3

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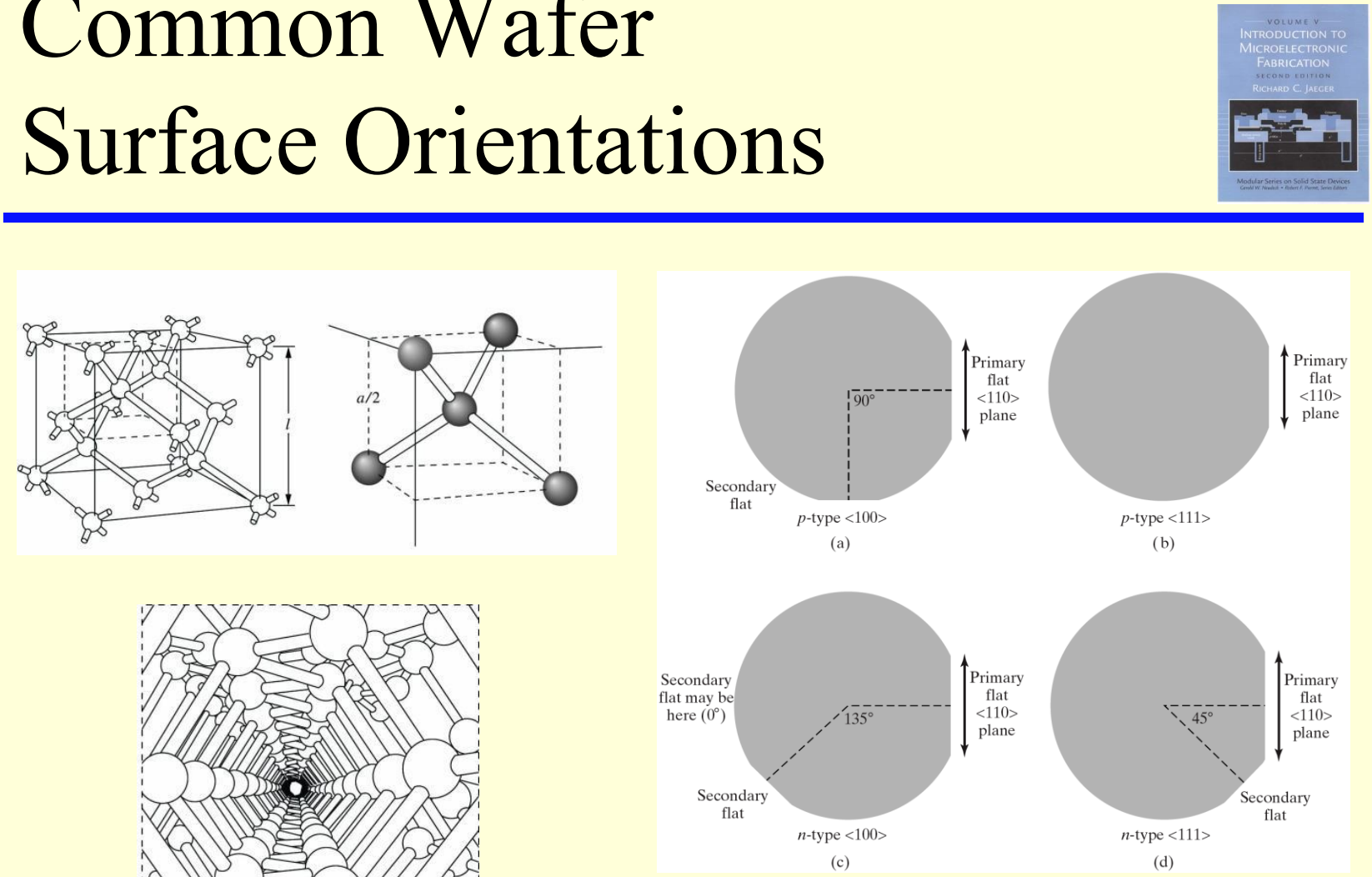
Common Wafer Surface Orientations



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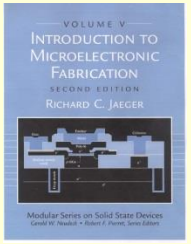
Wafer Cleaning



- Wafers must be cleaned of chemical and particulate contamination before photo processing
- Example of "RCA" cleaning procedure in table below

TABLE 2.2 Silicon Wafer Cleaning Procedure[4,5]

A. Solvent Removal
1. Immerse in boiling trichloroethylene (TCE) for 3 min.
2. Immerse in boiling acetone for 3 min.
3. Immerse in boiling methyl alcohol for 3 min.
4. Wash in DI water for 3 min.

B. Removal of Residual Organic/Ionic Contamination
1. Immerse in a (5:1:1) solution of H_2O–NH_4OH–H_2O_2; heat solution to 75–80 °C and hold for 10 min.
2. Quench the solution under running DI water for 1 min.
3. Wash in DI water for 5 min.

C. Hydrous Oxide Removal
1. Immerse in a (1:50) solution of HF–H_2O for 15 sec.
2. Wash in running DI water with agitation for 30 sec.

D. Heavy Metal Clean
1. Immerse in a (6:1:1) solution of H_2O–HCl–H_2O_2 for 10 min at a temperature of 75–80 °C.
2. Quench the solution under running DI water for 1 min.
3. Wash in running DI water for 20 min.

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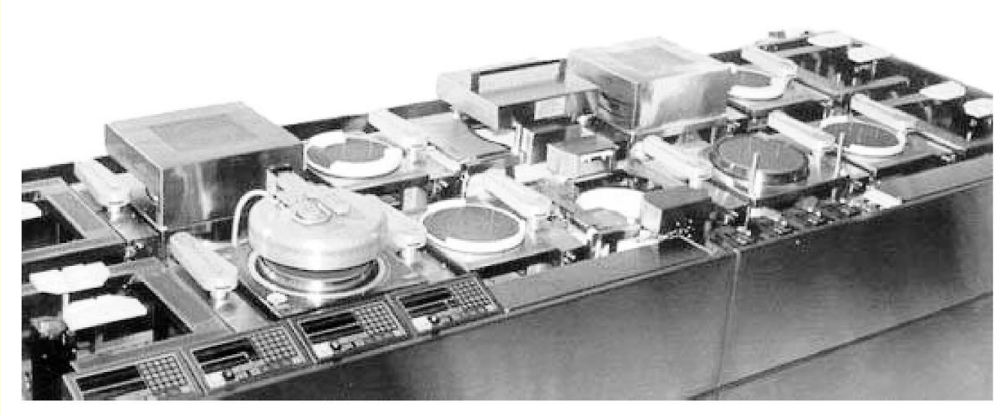
Photoresist Deposition
Automated Production Systems



- Rite Track 88e wafer processing system (Courtesy of Rite Track Services, Inc.

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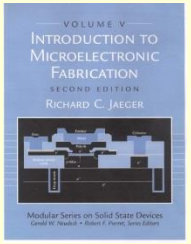
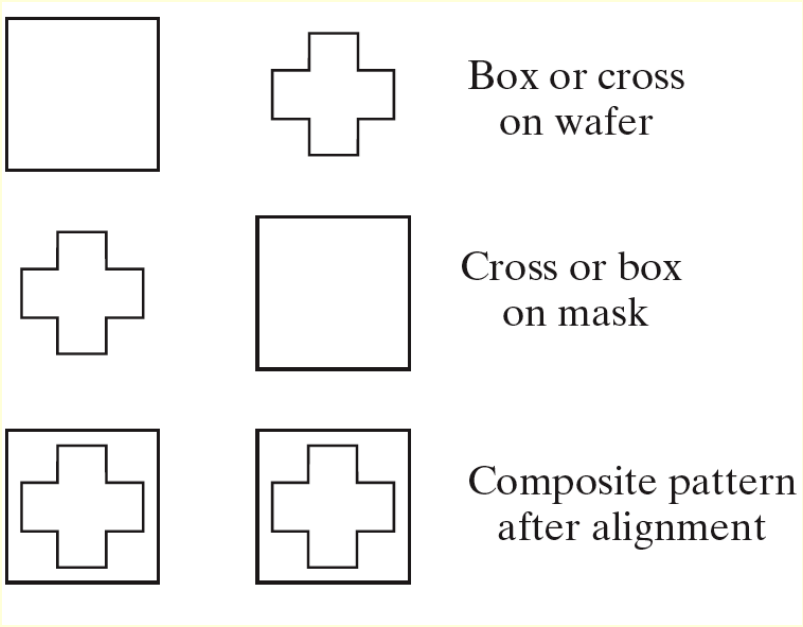
Mask Alignment





- Each mask must be carefully aligned to the previous levels
- Some form of alignment marks are used
- Automated alignment and exposure in production lines

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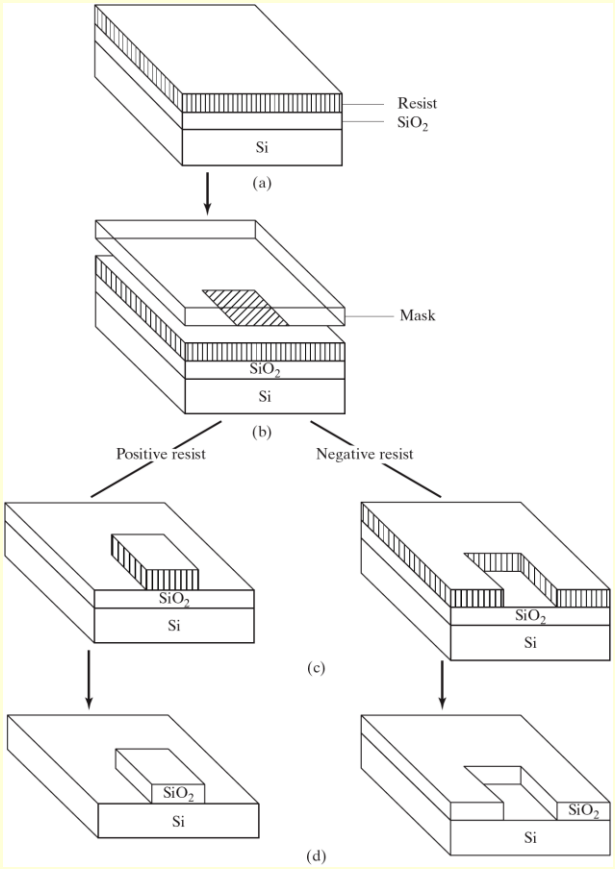
Resists for Lithography



- Resists
  - Positive
  - Negative
- Exposure Sources
  - Light
  - Electron beams
  - Xray sensitive

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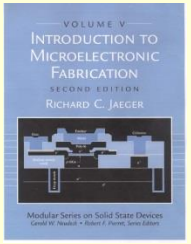
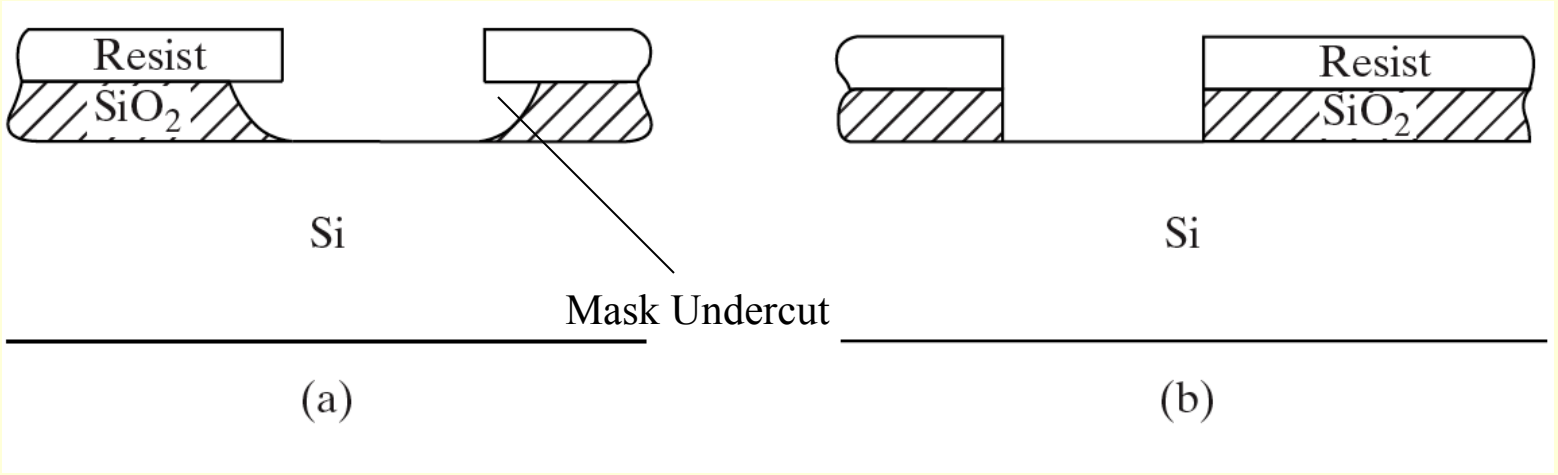
Oxide Etching Profiles



(a) Isotropic etching - wet chemistry - mask undercutting

(b) Anisotropic etching - dry etching in plasma or reactive ion etching system



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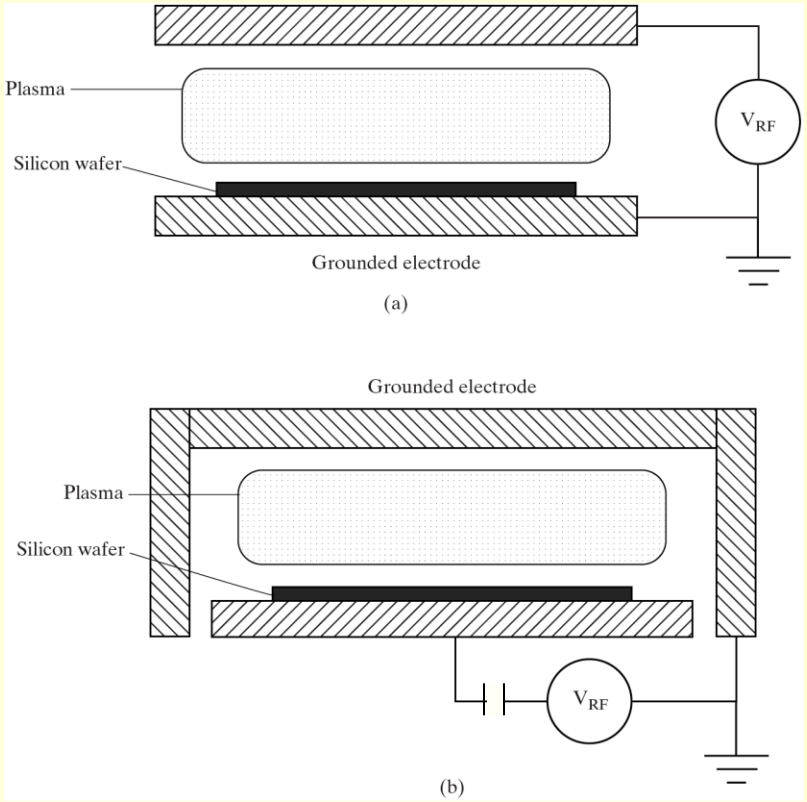
Dry Plasma Systems



(a) Conceptual drawing for a parallel plate plasma etching system

(b) Asymmetrical reactive ion etching (RIE) system

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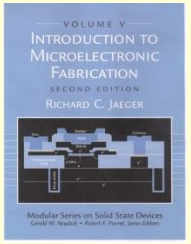
Plasma Etching Characteristics



- Anisotropic etching
- Minimizes chemical waste
- Etching
- Cleaning
- Resist removal "ashing"

TABLE 2.3 Etching Pressure Ranges

Etching Mode	Pressure (Torr)
Ion Milling	10^{-4}–10^{-3}
Reactive Ion Etching/Ion Milling	10^{-3}–10^{-1}
Plasma Etching	10^{-1}–5

1 atm = 760 mm Hg = 760 torr = 1.013 x 10^5 Pa 1 Pa = 1 N/m^2 = 0.0075 torr

TABLE 2.4 Plasma-Etching Sources

Material	Source Gases
Organic Materials	O_2, SF_6, CF_4
Polysilicon	CCl_4, CF_4, NF_3, SF_6
Silicon Dioxide	CF_4, C_2F_6, C_3F_8, CHF_3
Silicon Nitride	CF_4, C_2F_6, CHF_3, SF_6
Aluminum	CCl_4, Cl_2, BCl_3
Titanium	$C_2Cl_2F_4$, CF_4
Tungsten	Cl_2

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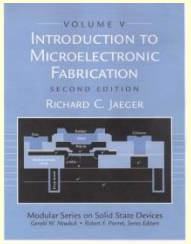
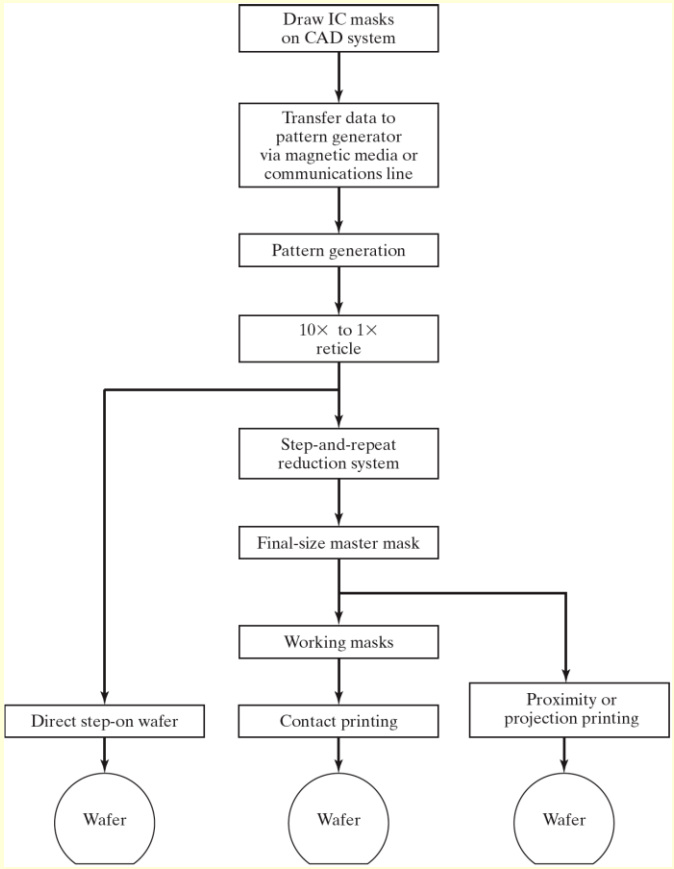
Mask Fabrication





- Masking processes
  - Direct step on wafer
  - Contact printing
  - Proximity printing
  - Projection printing

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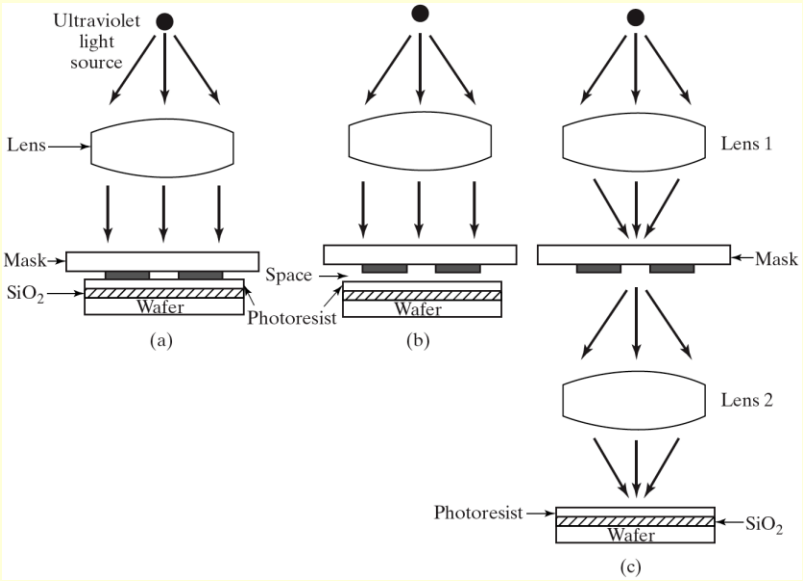
Printing Techniques



- Contact printing damages the reticle and limits the number of times the reticle can be used
- Proximity printing eliminates damage
- Projection printing can operate in reduction mode with direct step-on-wafer, eliminating the need for the reduction step presented earlier

FIGURE 2.11

Artist's conception of various printing techniques. (a) Contact printing, in which wafer is in intimate contact with mask; (b) proximity printing, in which wafer and mask are in close proximity; (c) projection printing, in which light source is scanned across the mask and focused on the wafer. Copyright, 1983, Bell Telephone Laboratories, Incorporated. Reprinted by permission from Ref. [5].

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Wafer Steppers

Figure 2.13 The true complexity of a wafer stepper is apparent in this system drawing. (Courtesy of ASM Lithography, Inc.

- Wafer stepping systems widely used
- Must be completely isolated from sources of vibration
- High degree of environmental control needed
- Often in their own clean room

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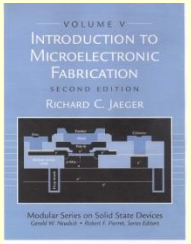
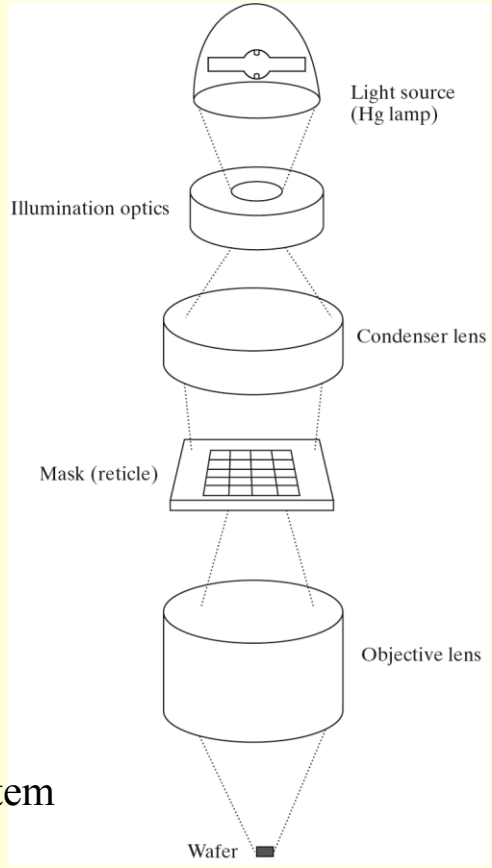
Wafer Steppers (cont.)





Lens System

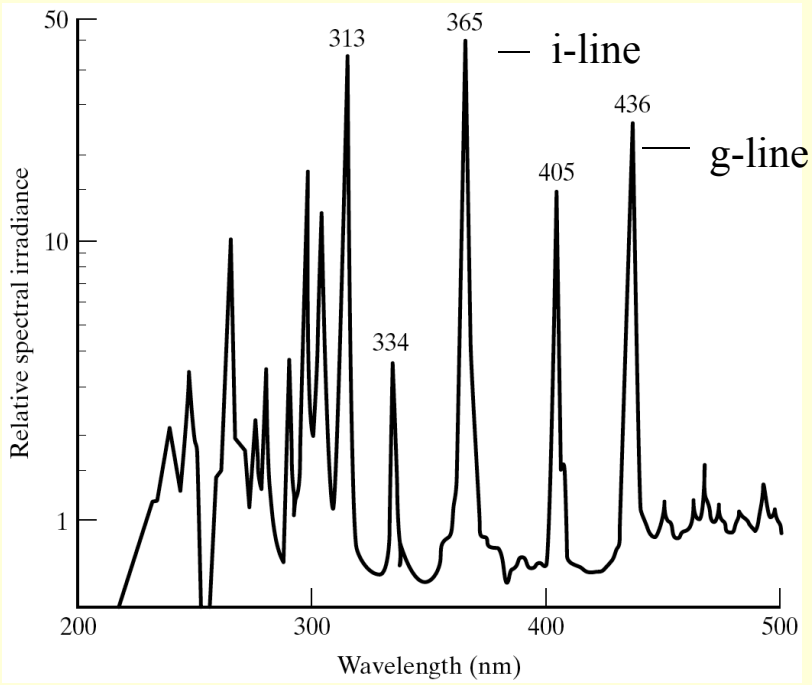
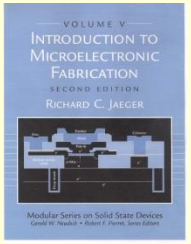
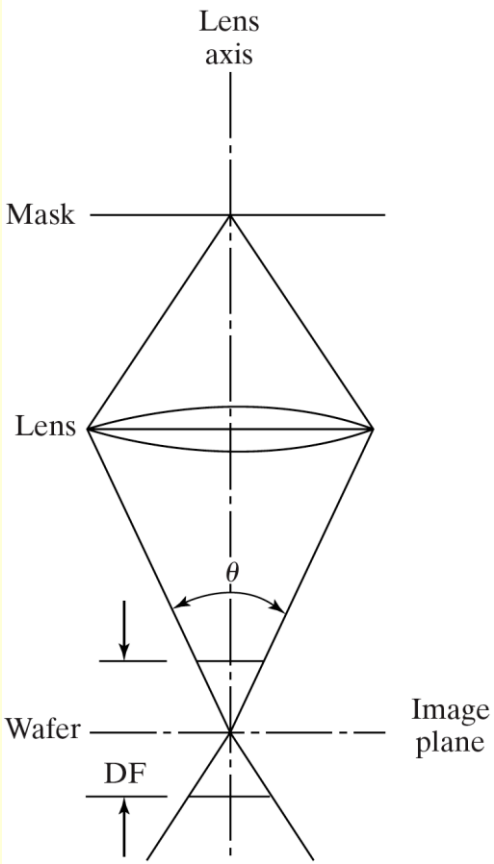


Figure 2.15
Spectral Content of Xe-Hg lamp (Courtesy of SVG)

Minimum Feature Size and Depth of Field





$$\text{Minimum Feature Size } F = 0.5\frac{\lambda}{NA}$$

$$\text{Depth of Field DF} = 0.6\frac{\lambda}{(\text{NA})^2}$$

$$\text{Numerical Aperture } NA = \sin\theta$$

$$\lambda = \text{wavelength of exposure source}$$

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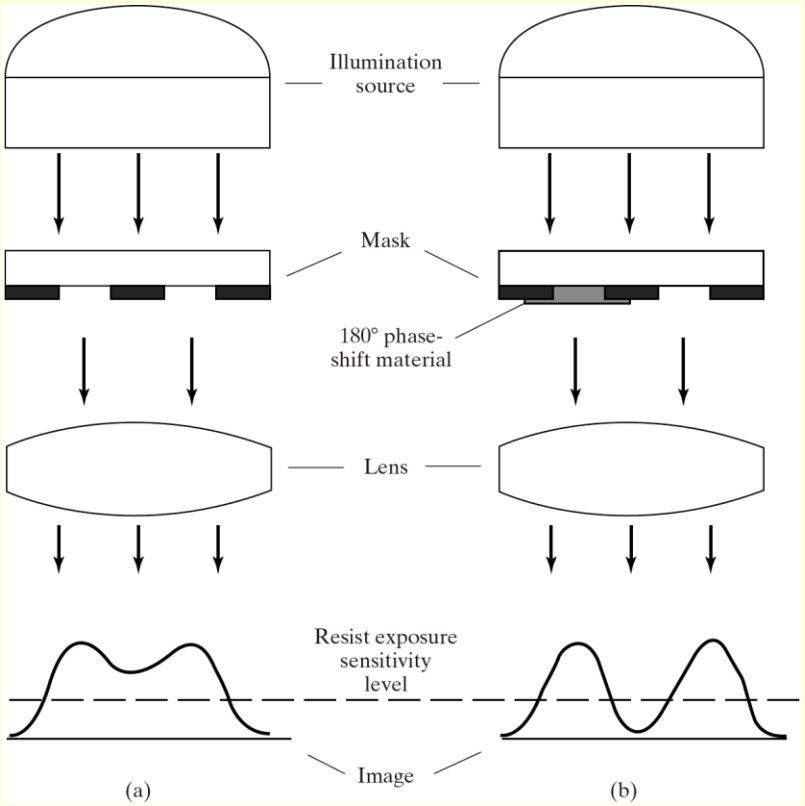
Phase Shifting Masks



Pattern transfer of two closely spaced lines

(a) Conventional mask technology - lines not resolved

(b) Lines can be resolved with phase-shift technology

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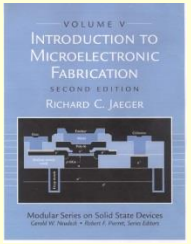
ITRS Lithography Projections



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DUV - deep ultraviolet; EUV - extreme ultraviolet; PSM - phase shift mask;

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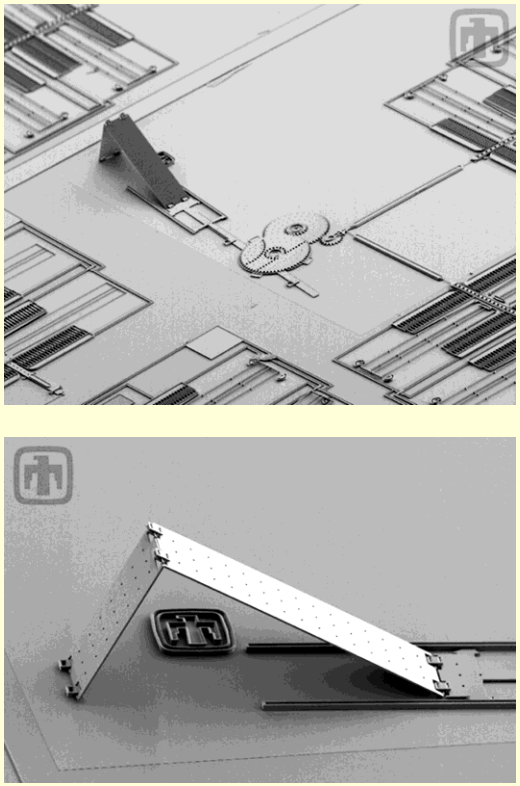
Inspection
SEM, TEM, STM



SEM images of a three-dimensional micro-electro-mechanical system (MEMS) structure (Courtesy of Sandia National Laboratories).

"A picture is worth a thousand words"

- Optical microscopy
- Scanning electron microscopy (SEM)
- Transmission electron microscopy (TEM)
- Scanning tunneling microscopy (STM)

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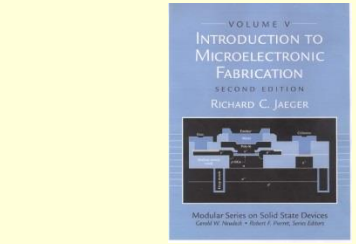
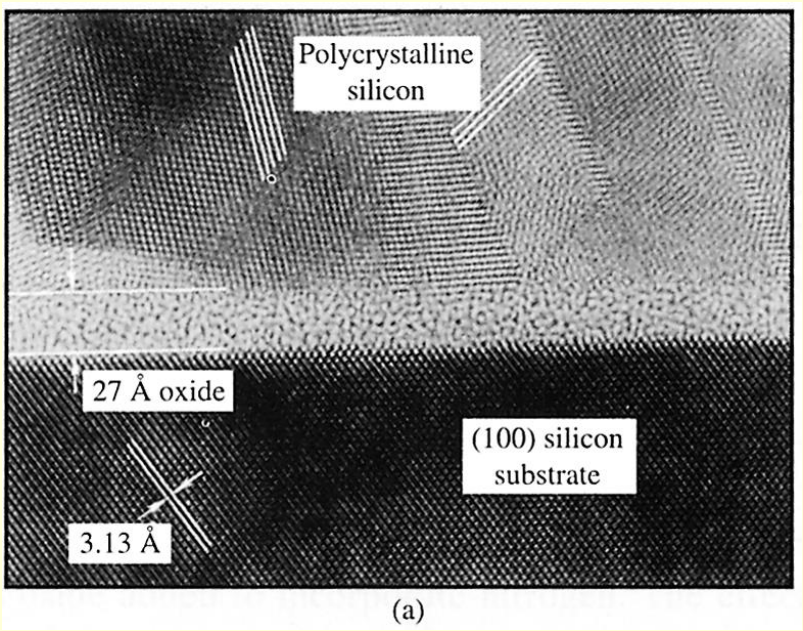
Inspection
TEM





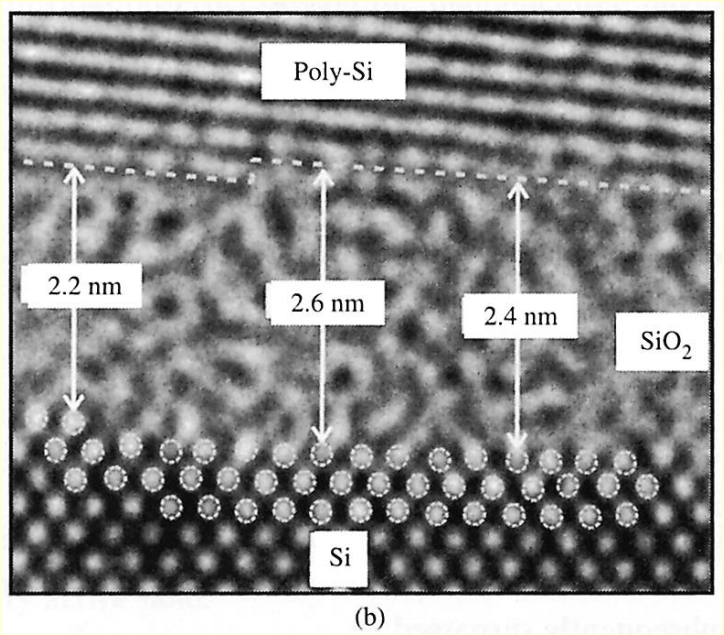
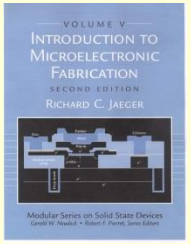
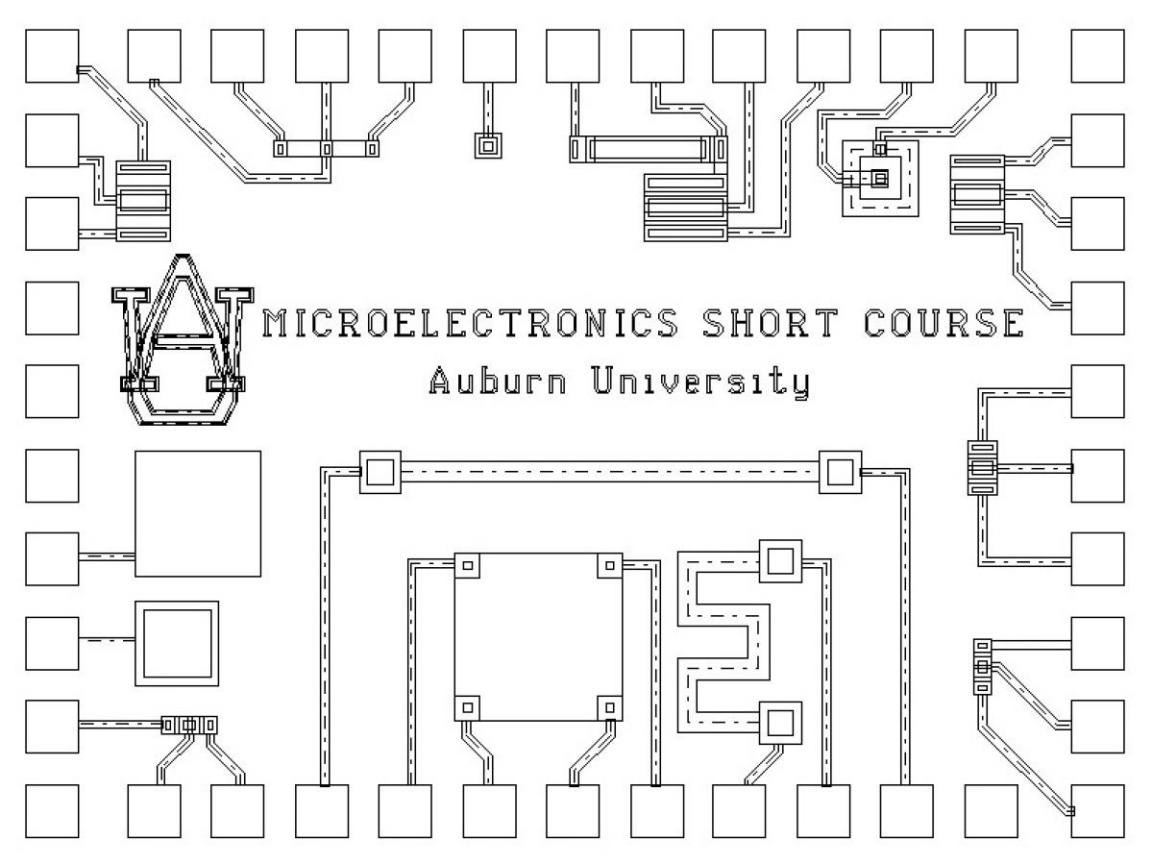


Figure 2.18
Cross-sectional high-resolution TEM images for MOS structures with (a) 27-Å and (b) 24-Å Image. Polysilicon grains are easily noticeable in (a); the Si/SiO2 and poly-Si/SiO2 interfaces are shown in part (b). On a local atomic scale, thickness variations of 2-3 Å are found which are a direct result of atomic steps at both interfaces. Copyright 1969 by International Business Machines Corporation; reprinted with permission from Ref. [9].

Layout of a Class Chip





Basic 4-Mask Process

PMOS Metal-Gate Process

1. p-diffusion
2. Thin oxide
3. Contacts
4. Metal

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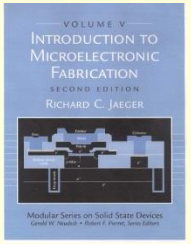
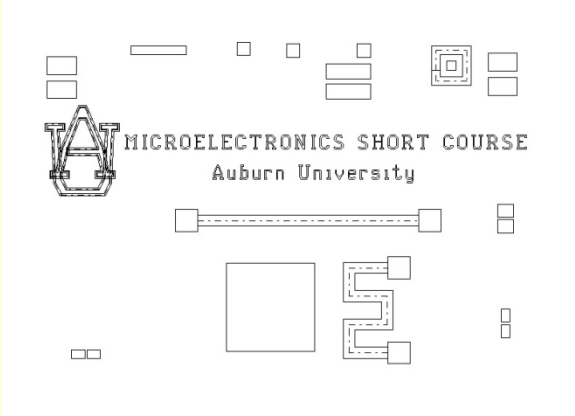
Four Mask Class Process

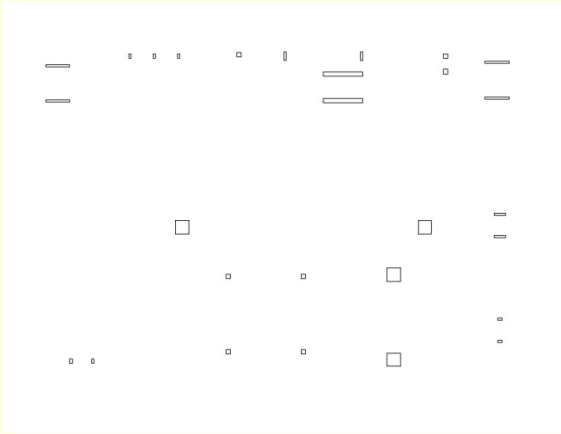


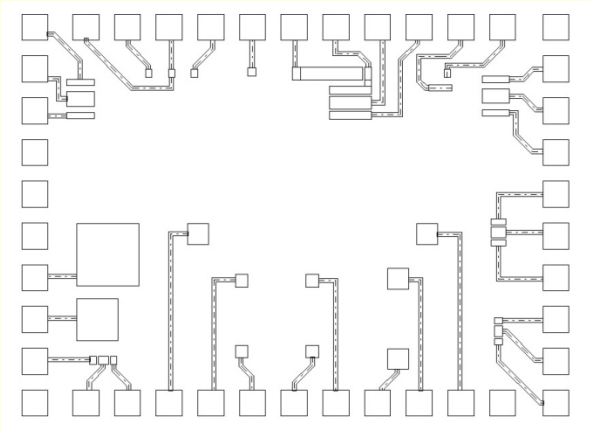
p-diffusion



Thin oxide

Contacts





Metal

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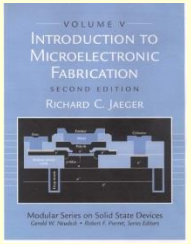
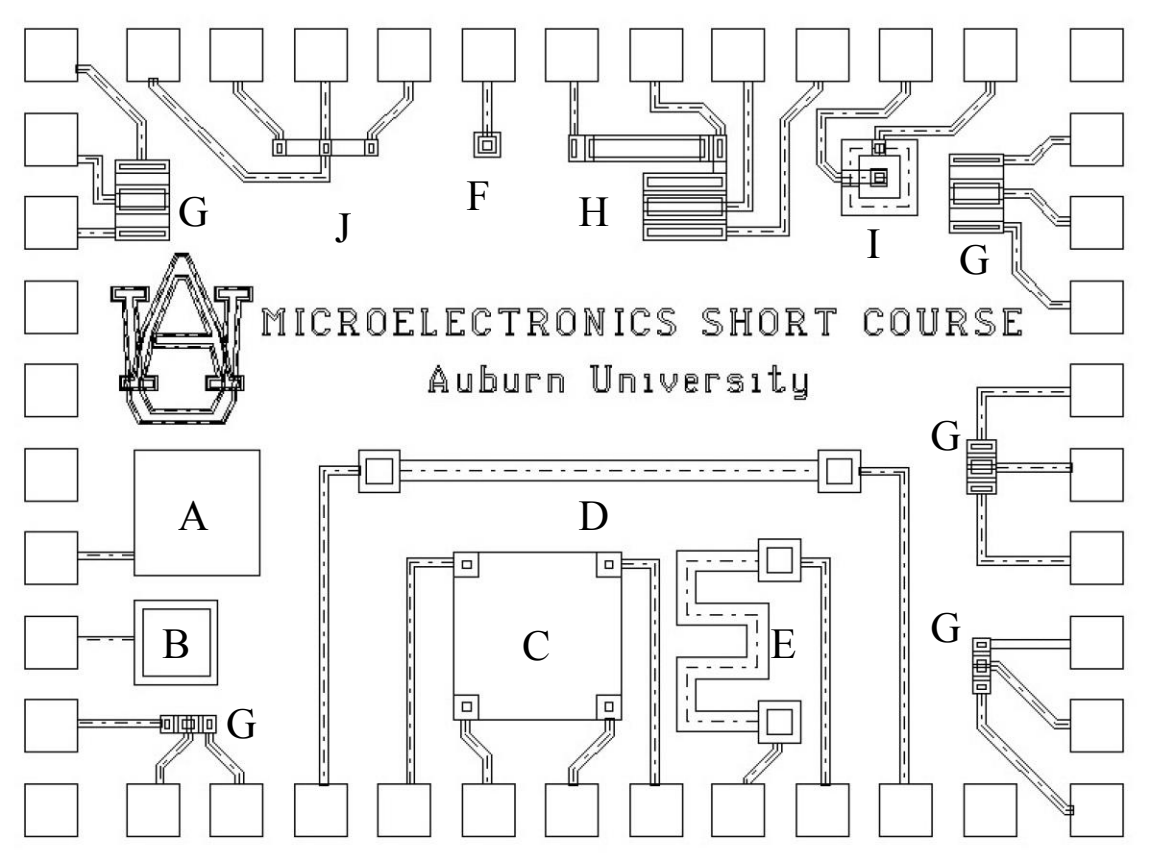
Layout of Class Chip





Metal Gate PMOS Process

A. Thick oxide capacitor
B. Thin Oxide Capacitor
C. Van der Pauw structure
D. Resistor 1
E. Resistor 2
F. Diode
G. PMOS transistors
H. PMOS logic inverter
I. Lateral pnp transistor
J. Kelvin contact structure

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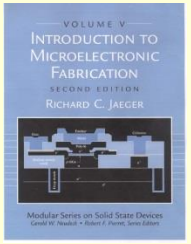
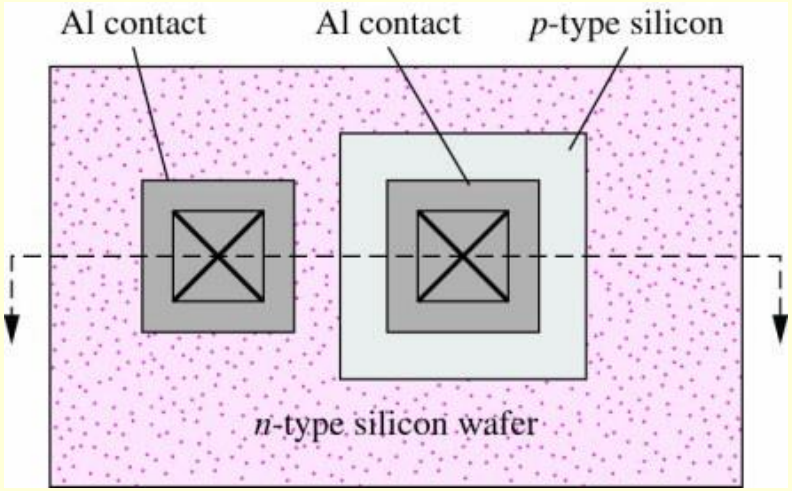
Our Class Process
Diode & Resistor Fabrication





Top view of an integrated pn diode.

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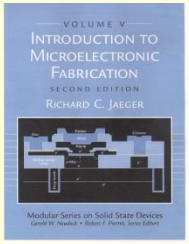
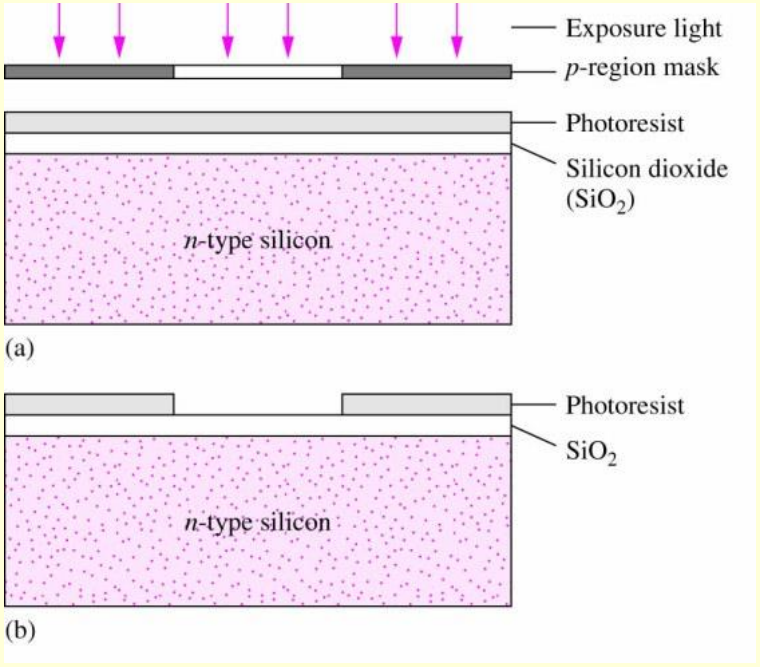
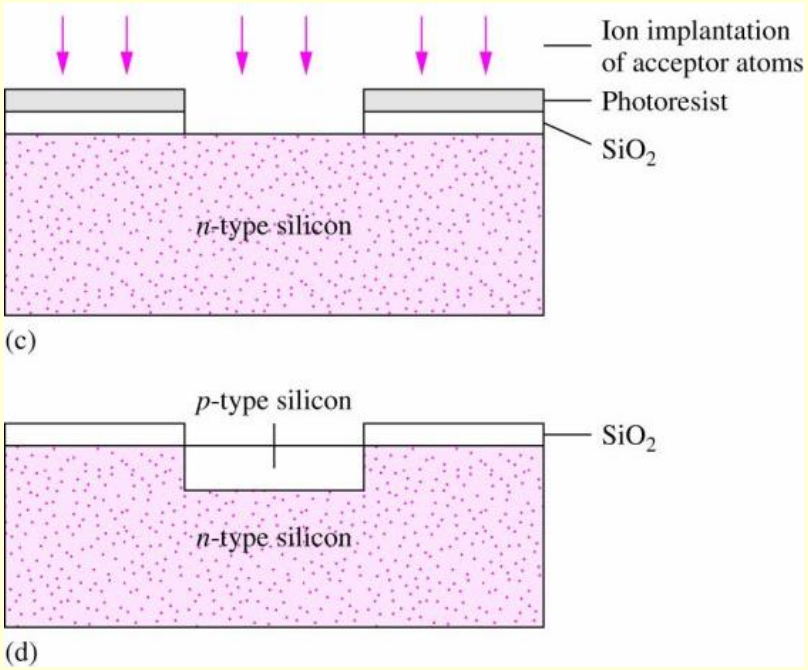
Our Class Process
Diode Fabrication (cont.)







(a) First mask exposure (b) Post-exposure and development of photoresist
(c) After SiO_2 etch (d) After implantation/diffusion of acceptor dopant.

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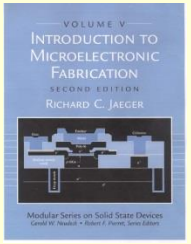
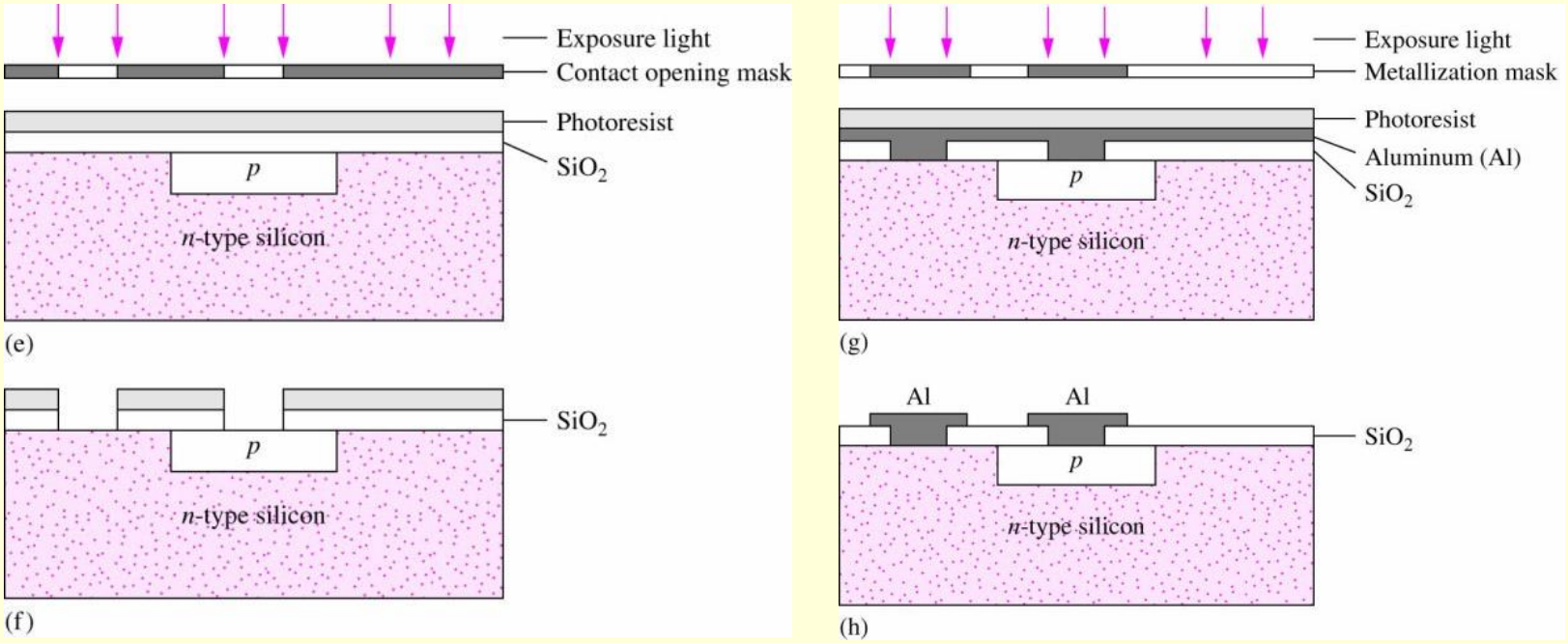
Our Class Process
Diode Fabrication (cont.)





(e) Exposure of contact opening mask, (f) after resist development and etching of contact openings, (g) exposure of metal mask, and (h) After etching of aluminum and resist removal.

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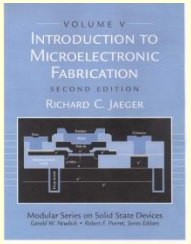
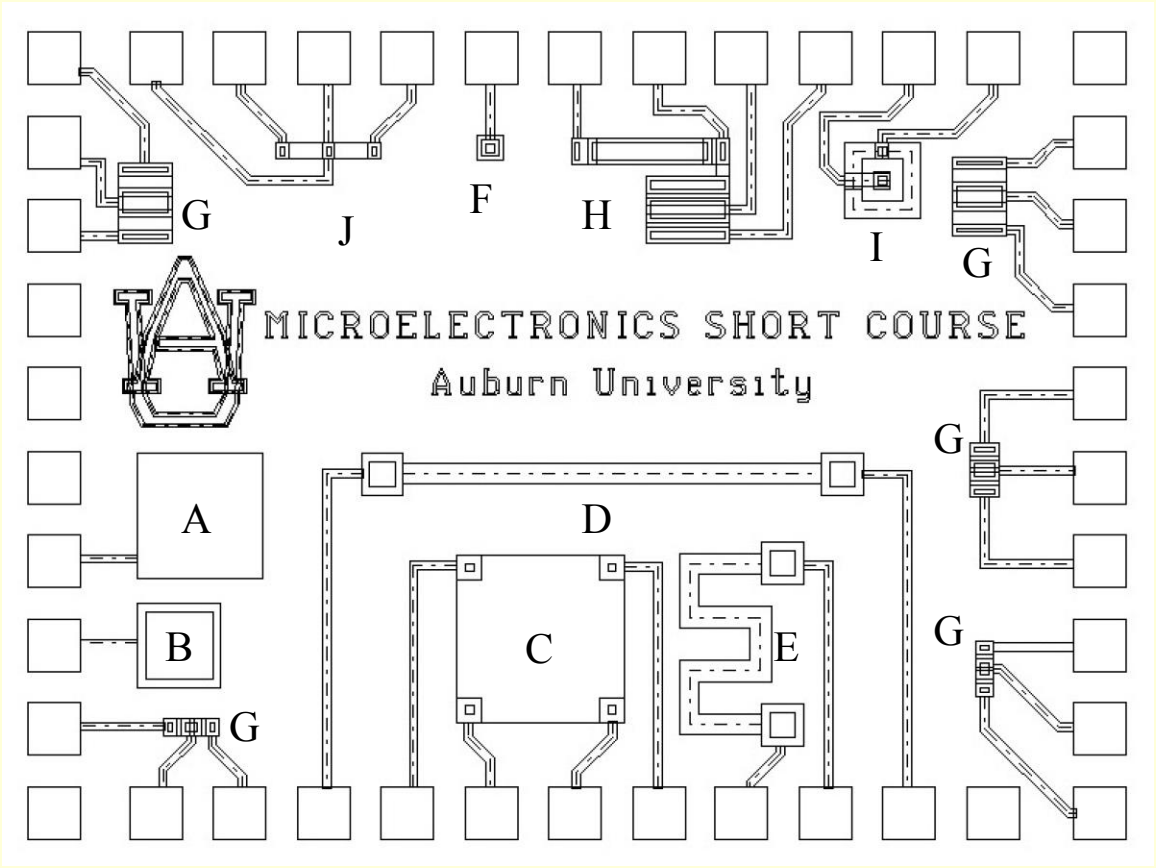
Layout of Class Chip





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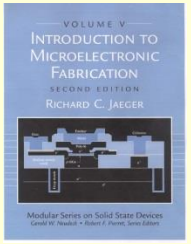
References



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End of Chapter 2

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