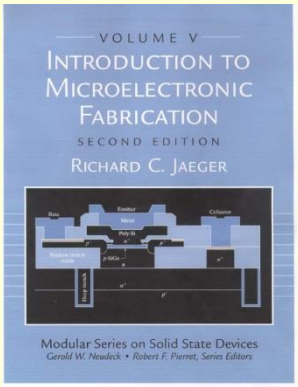
Introduction to Microelectronic Fabrication

Chapter 1
An Overview of Microelectronic Fabrication



Historical Trends
Silicon Wafer Size

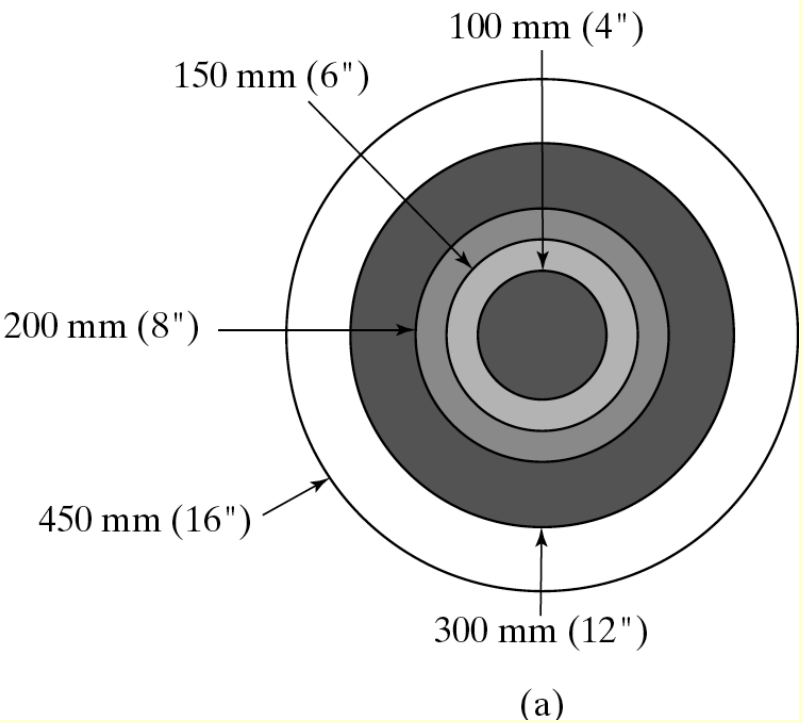


FIGURE 1.1

(a) Relative size of wafers with diameters ranging from 100 to 450 mm; (b) The same integrated circuit die is replicated hundreds of times on a typical silicon wafer; (c) the graph gives the approximate number of 10 x 10 mm dice that can be fabricated on wafers of different diameters.

- Early Wafers - 1, 1.5, 2 Inch Diameters
- Wafer Size has Increased Steadily
- 200 mm (8") Wafers in Production
- 300 mm (12") Coming on Line Now (> 3B$/Fab)
- 450 mm Planned

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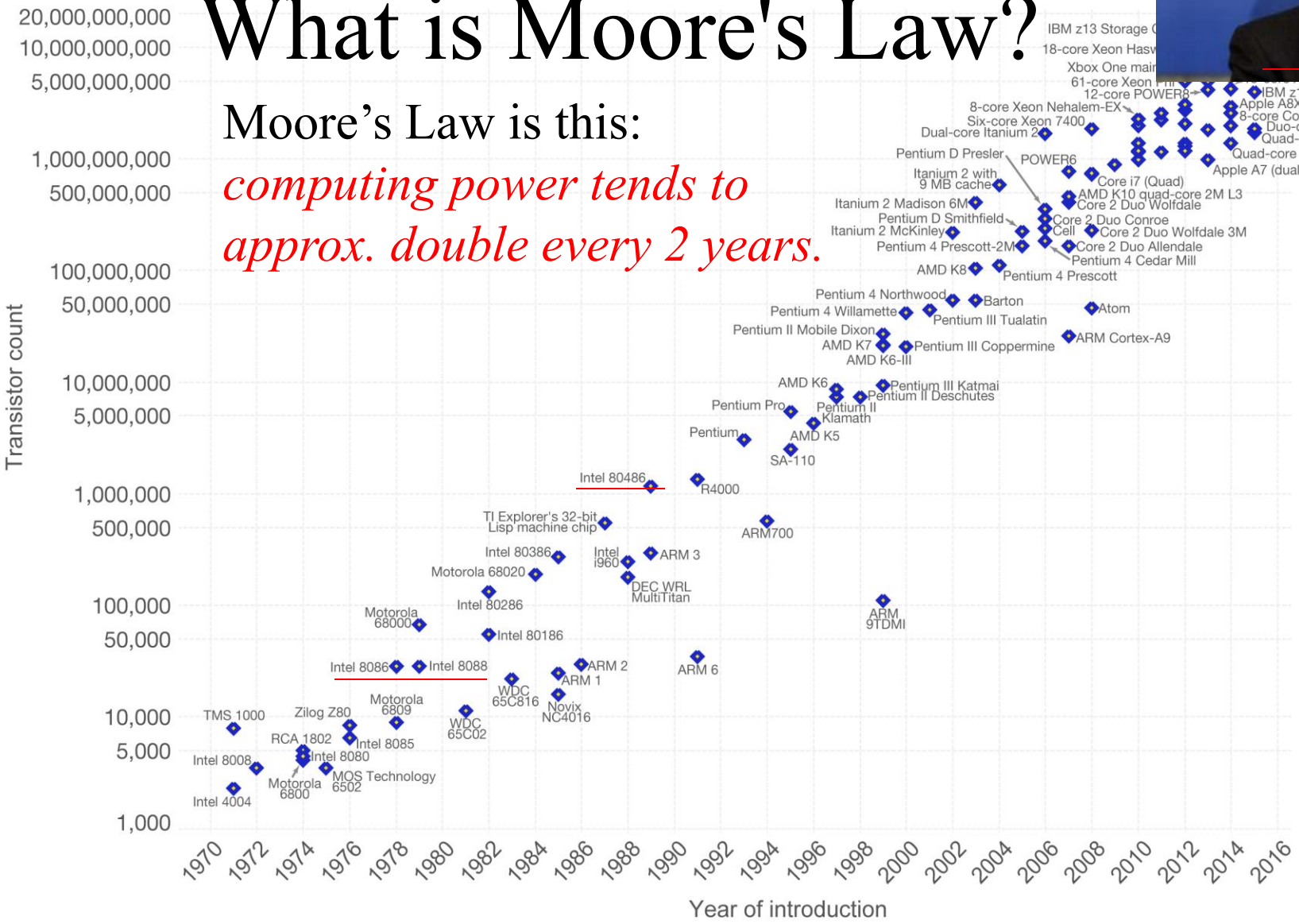
Moore's Law – The number of transistors on integrated circuit chips

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approxi
This advancement is important as other aspects of technological progress – such as processing speed or the price of
strongly linked to Moore's law.

What is Moore's Law?

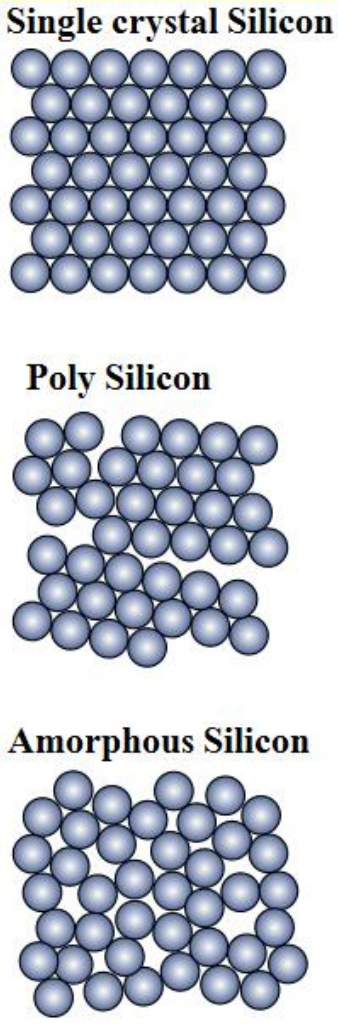
Moore's Law is this:

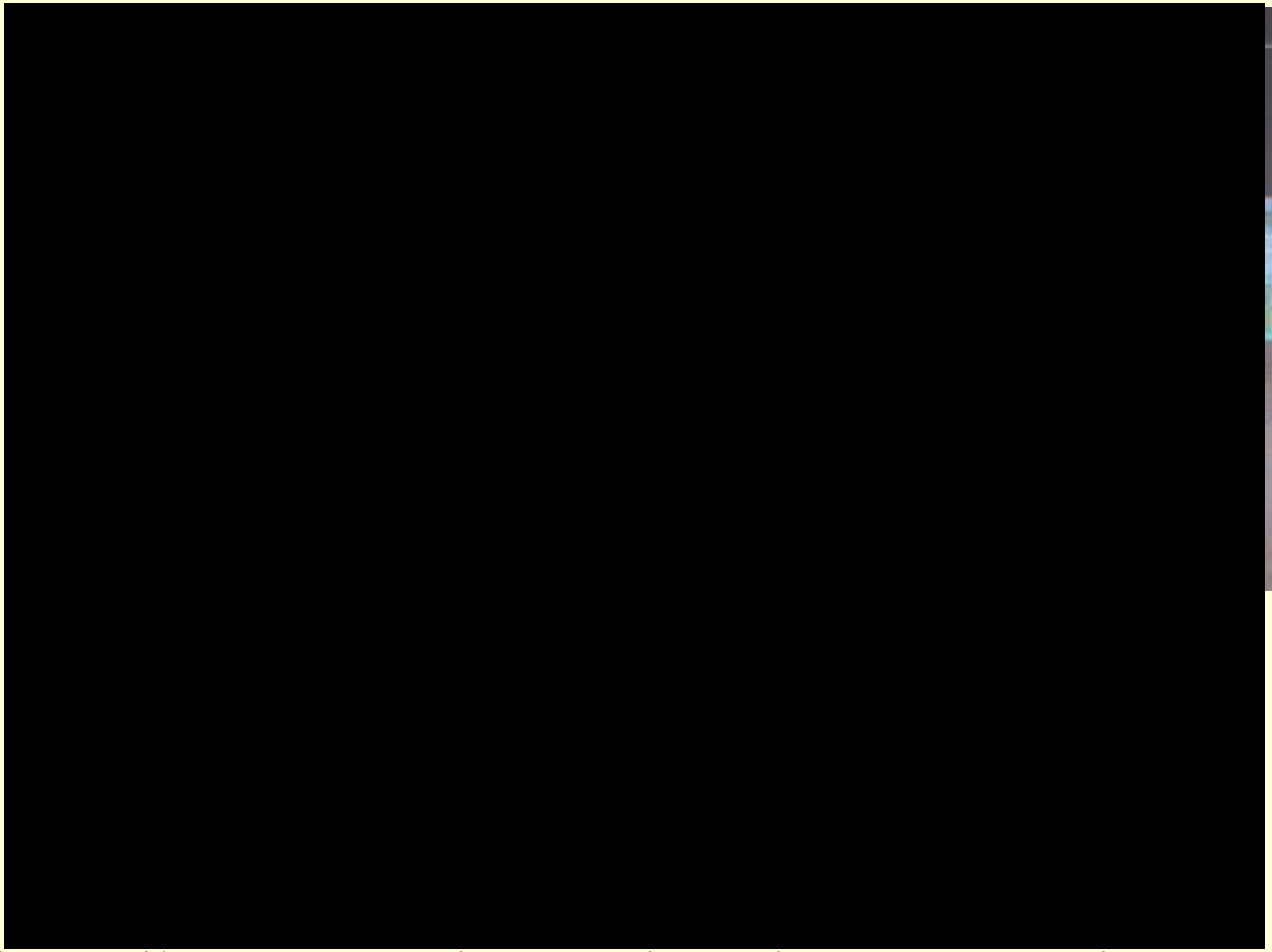
computing power tends to approx. double every 2 years.



Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

How do they make Silicon Wafers and Computer Chips

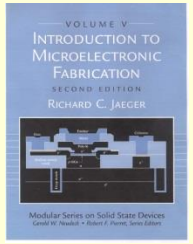


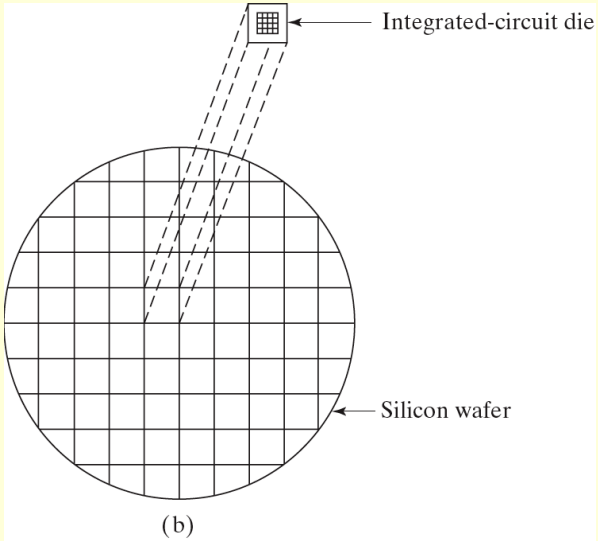


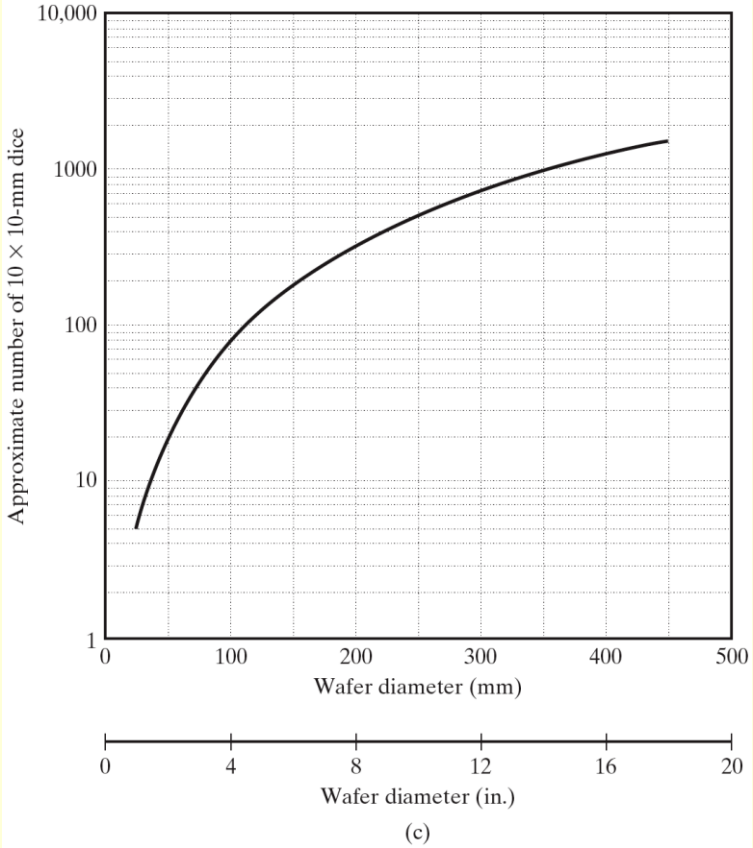
Silicon ingot

https://www.youtube.com/watch?v=aWVywhzuHnQ

Larger Wafers
Lower Die Cost







- Cost to Process a Wafer is Relatively Fixed for a Given Process
- Larger Wafer →Lower Cost/Die

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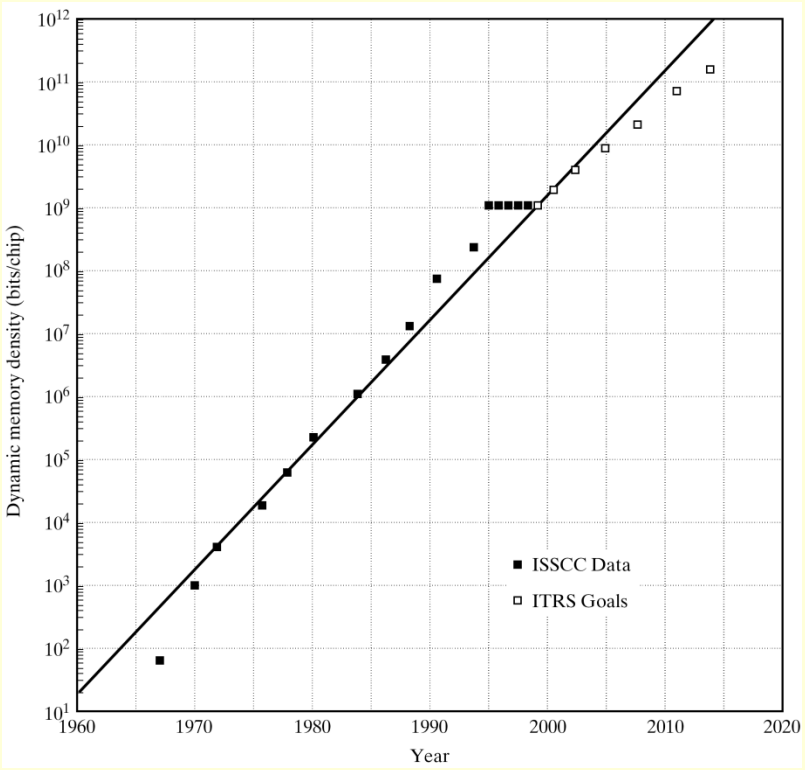
Historical Trends
Memory Density (Bits/Chip)



- Moore's Law - Exponential Increase in Chip Complexity
- ISSCC Research Benchmarks
  - 1967 - 64 bit Memory
  - 1984 - 1Mb Memory
  - 1995 - First 1 Gb Memory

FIGURE 1.2
(a) Dynamic memory density versus year since 1960.

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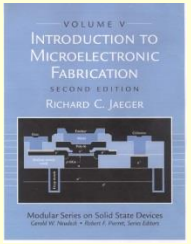
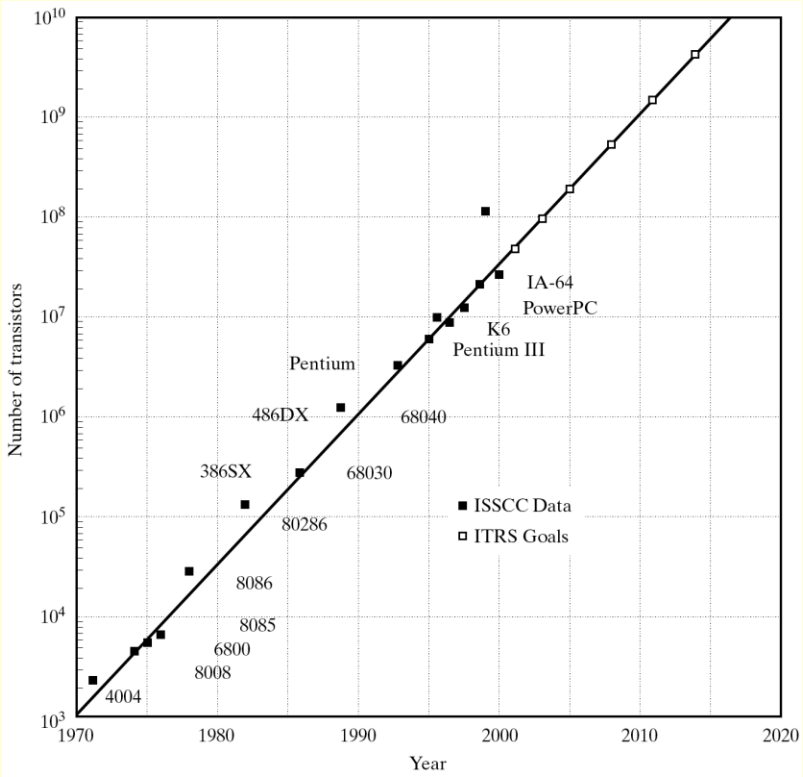
Historical Trends

Microprocessor Complexity (Trans./Chip)



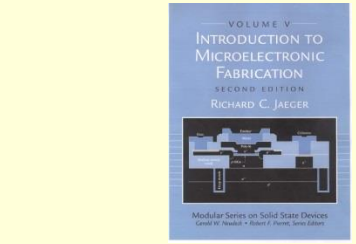


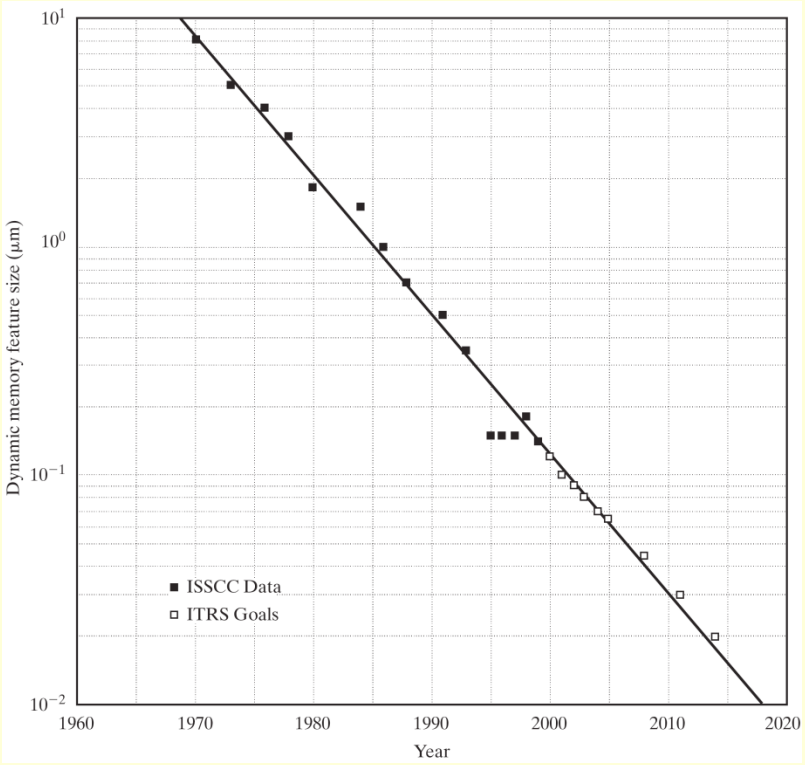
- ISSCC Benchmarks
  - 1971 - 2000 Transistors
  - 1988 - 1M Transistors
  - 1998 - 100M Transistors

FIGURE 1.2

(b) Number of transistors in a microprocessor versus year.

Historical Trends
Memory Feature Size (μm)





- Feature Size Decreases by 2X approximately every 5 years
- Each New Process Generation Doubles Density - Reduction of Feature Size by 0.707
- The Original Nanotechnology!
  - Feature size now 70-90 nm
- Transistors Operate Normally

FIGURE 1.3

Feature size used in fabrication of dynamic memory as a function of time.

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Semiconductor Industry Roadmap - ITRS

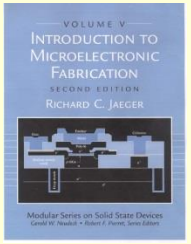

TABLE 1.1 International Technology Road Map for Semiconductors (ITRS) [4]

	Selected Projections					
Year of First Product Shipment	2001	2003	2005	2008	2011	2014
DRAM Metal Line Half-Pitch (nm)	150	120	100	70	50	35
Microprocessor Gate Widths (nm)	100	80	65	45	30	20
DRAM (G-bits/chip)	2.2	4.3	8.6	24	68	190
Microprocessor (M-transistors/chip)	48	95	190	540	1500	4300
DRAM Chip Area: Year of Introduction (mm^2)	400	480	526	600	690	790
DRAM Chip Area: Production (mm^2)	130	160	170	200	230	260
MPU Chip Size at Introduction (mm^2)	340	370	400	470	540	620
MPU Chip Area: Second "shrink" (mm^2)	180	210	230	270	310	350
Wafer Size (mm)	300	300	300	450	450	450

[4] *The International Technology Roadmap for Semiconductors*, The Semiconductor Industry Association (SIA), San Jose, CA, 1999. (http://www.semichips.org)

Each new process generation doubles chip density by scaling feature size by 0.7.

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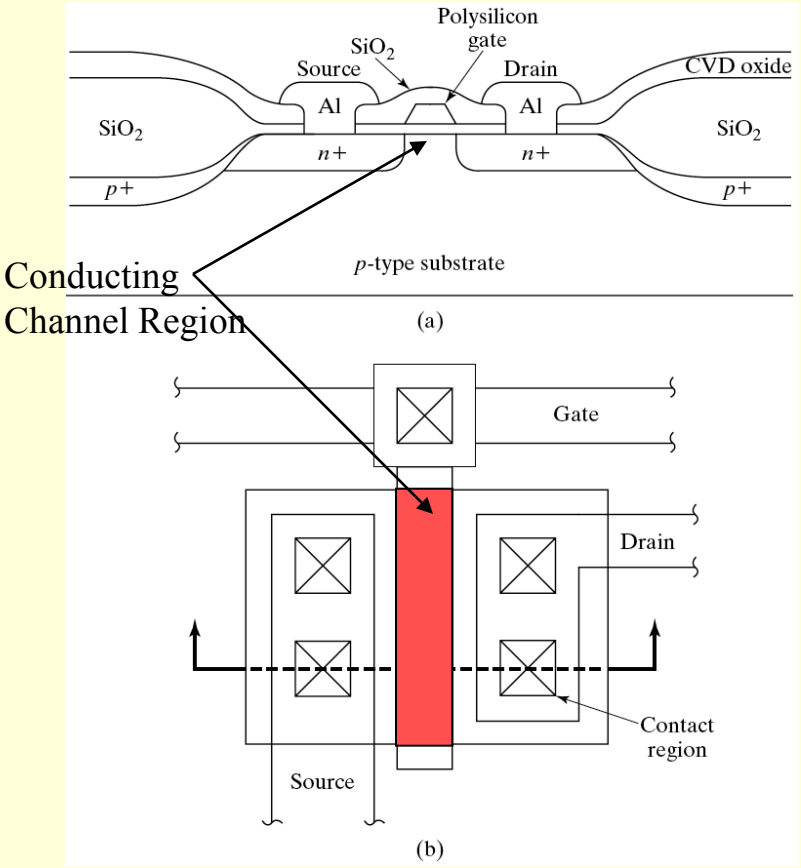
NMOS Transistor

Top View and Cross-Section

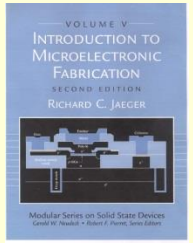


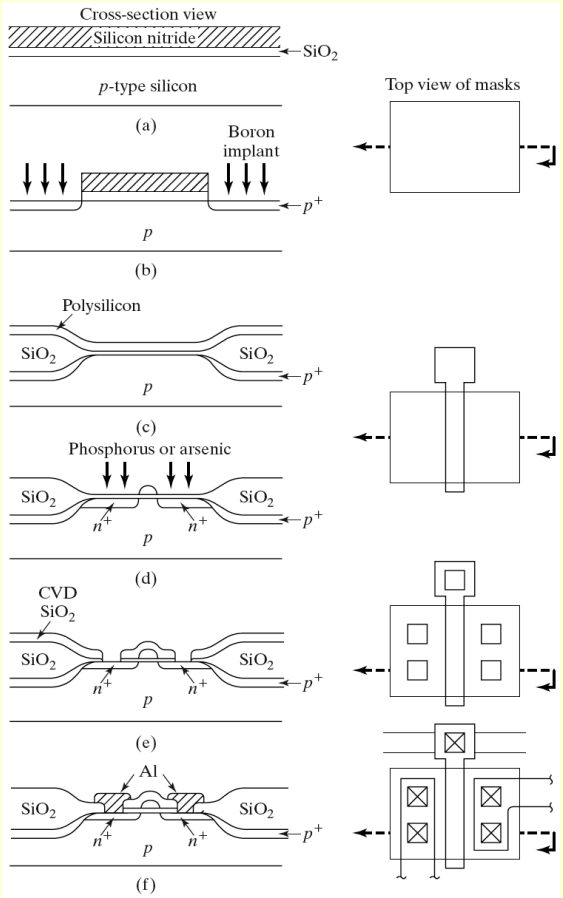
- N-Channel Metal-Oxide Semiconductor Transistor
- n- and p-type semiconductor regions
- Thick and thin oxides
- Etching Openings
- Polysilicon gate
- Metal (Al) Interconnections

FIGURE 1.4

The basic structure of an *n*-channel metal-oxide-semiconductor (NMOS) transistor structure. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a). The transistor uses heavily doped polysilicon as the gate "metal."

Basic NMOS Process
Key Steps

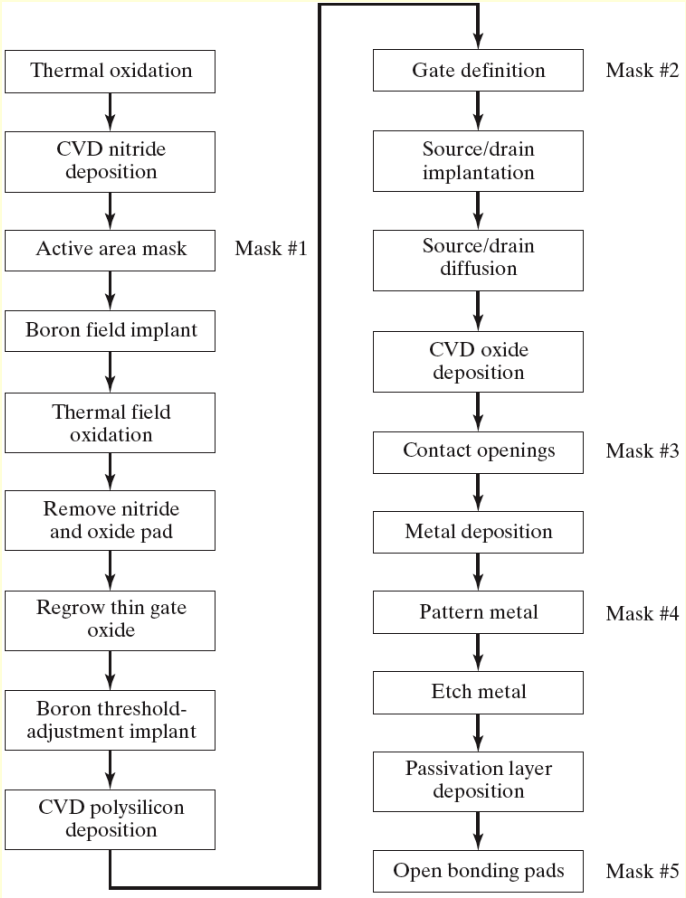




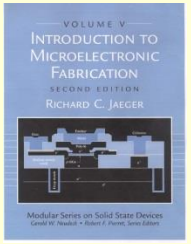
- Oxidation
- Photolithography
- Implantation
- Diffusion
- Etching
- Film Deposition

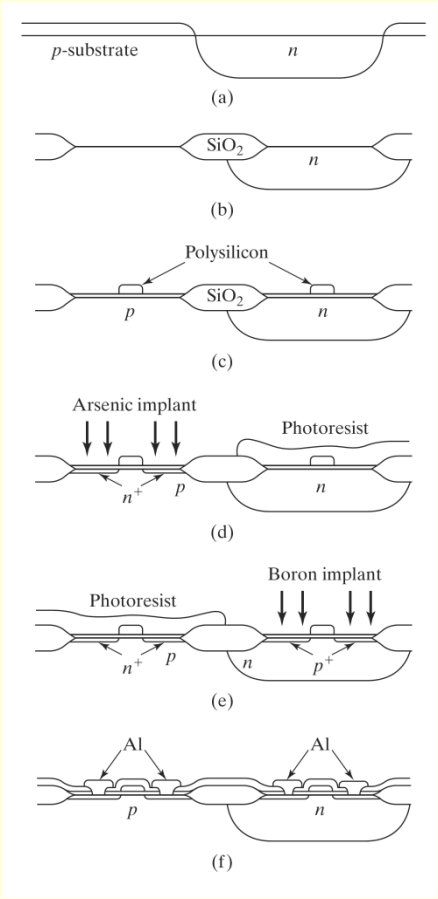
FIGURE 1.6

Process sequence for a semirecessed oxide NMOS process. (a) Silicon wafer covered with silicon nitride over a thin padding layer of silicon dioxide; (b) etched wafer after first mask step. A boron implant is used to help control field oxide threshold; (c) structure following oxidation, nitride removal, and polysilicon deposition; (d) wafer after second mask step and etching of polysilicon; (e) the third mask has been used to open contact windows following silicon dioxide deposition; (f) final structure following metal deposition and patterning with fourth mask.



CMOS Technology
N-Well Technology Cross-Section





Oxidation

Photolithography

Implantation

Diffusion

Etching

Film Deposition

- Complementary Metal-Oxide Semiconductor Technology
- Dominant Technology in Integrated Circuits Today!
- Requires both NMOS and PMOS Transistors

FIGURE 1.8

Cross-sectional views at major steps in a basic CMOS process. (a) Following *n*-well diffusion, (b) following selective oxidation, and (c) following gate oxidation and polysilicon gate definition; (d) NMOS source/drain implantation; (e) PMOS source/drain implantation; (f) structure following contact and metal mask steps.

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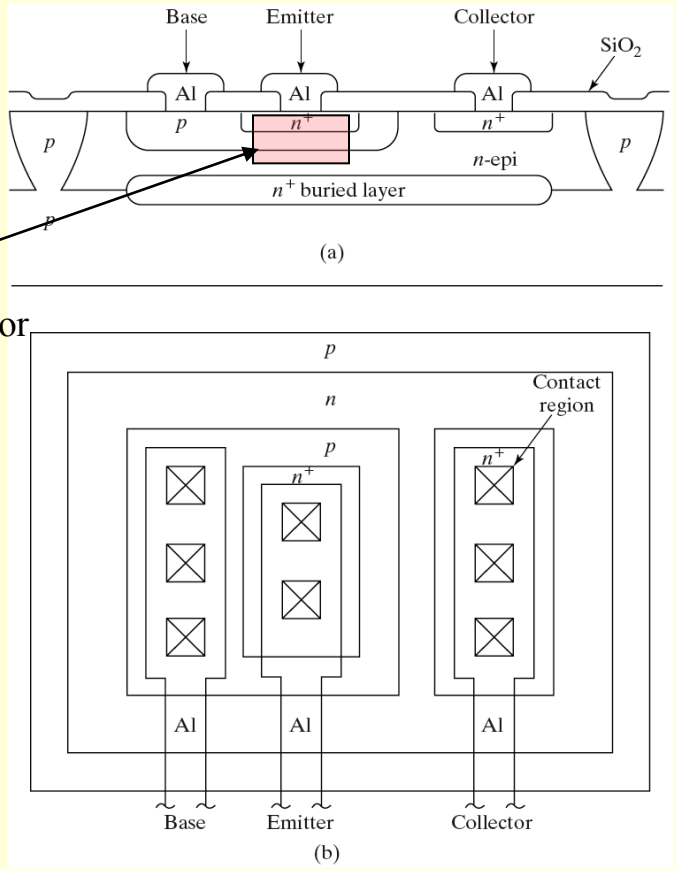
Bipolar Transistor
Top View and Cross-Section



- Bipolar Junction Transistor (BJT)
- Standard Buried Collector Process (SBC)
- n- and p-type semiconductor regions
- Thick and thin oxides
- Etching Openings
- Metal (Al) Interconnections

FIGURE 1.5

The basic structure of a junction-isolated bipolar transistor. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a).

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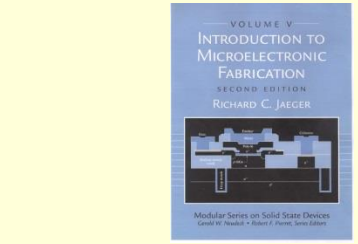
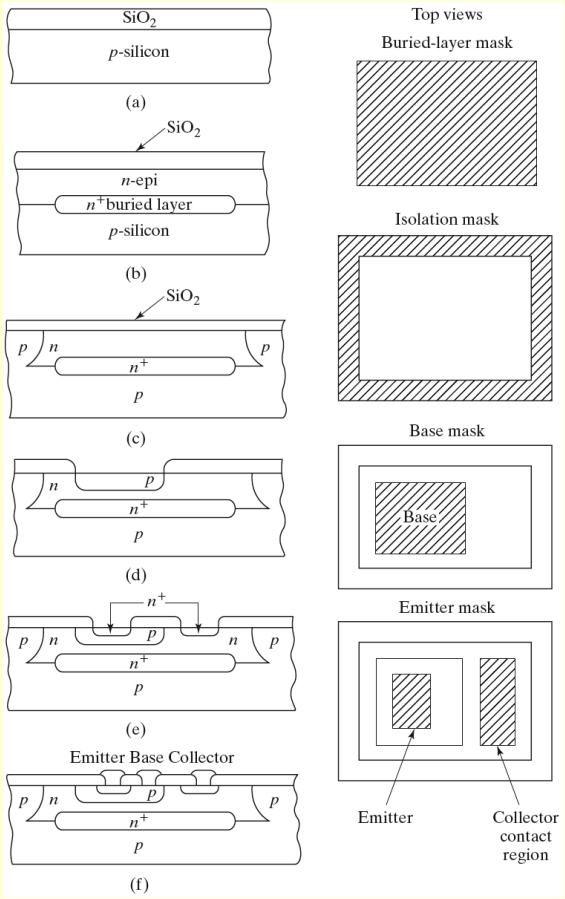
SBC Process
Key Steps

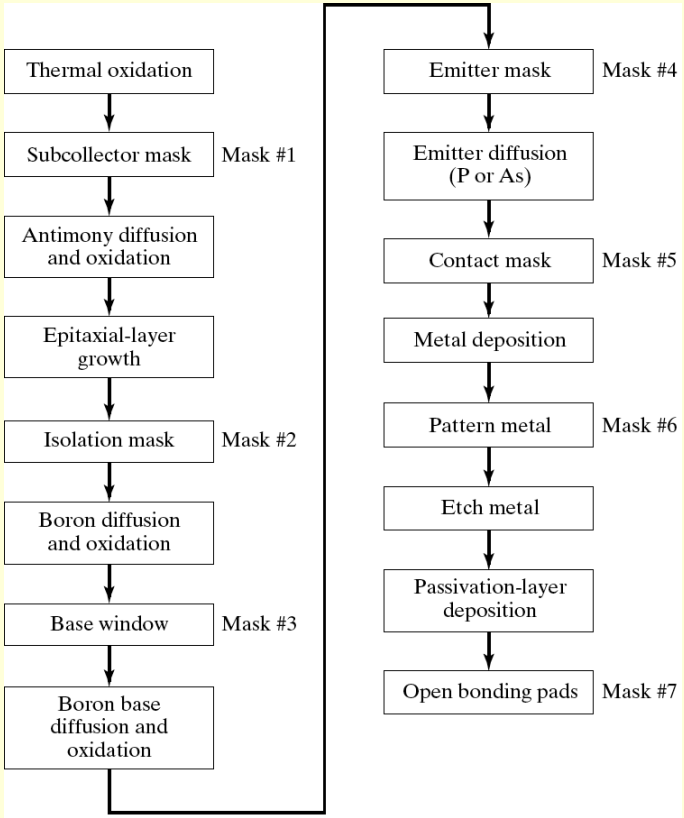




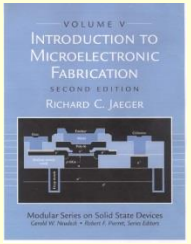
- Oxidation
- Photolithography
- Implantation
- Diffusion
- Etching
- Film Deposition

FIGURE 1.9

Cross-sectional view of the major steps in a basic bipolar process. (a) Wafer with silicon dioxide layer; (b) following buried-layer diffusion using first mask, and subsequent epitaxial layer growth and oxidation; (c) following deep-isolation diffusion using second mask; (d) following boron-base diffusion using third mask; (e) fourth mask defines emitter and collector contact regions; (f) final structure following contact and metal mask steps.



References



[1] *Digest of the IEEE International Solid-State Circuit Conference*, held in February of each year. (http://www.sscs.org/isscc)

[2] *Digest of the IEEE International Electron Devices Meeting*, held in December of each year. (http://www.ieee.org/conference/iedm)

[3] *Digests of the International VLSI Technology and Circuits Symposia*, co-sponsored by the IEEE and JSAP, held in June of each year. (http://www.vlsisymposium.org)

[4] *The International Technology Roadmap for Semiconductors*, The Semiconductor Industry Association (SIA), San Jose, CA, 1999. (http://www.semichips.org)

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End of Chapter 1

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