Introduction to Microelectronic Fabrication

Chapter 1
An Overview of Microelectronic Fabrication
Historical Trends
Silicon Wafer Size

- Early Wafers - 1, 1.5, 2 Inch Diameters
- Wafer Size has Increased Steadily
- 200 mm (8”) Wafers in Production
- 300 mm (12”) Coming on Line Now (> 3B$/Fab)
- 450 mm Planned
Moore's Law is this: computing power tends to approx. double every 2 years.
How do they make Silicon Wafers and Computer Chips

Single crystal Silicon

Poly Silicon

Amorphous Silicon

https://www.youtube.com/watch?v=aWVywhzuHnQ
Larger Wafers
Lower Die Cost

• Cost to Process a Wafer is Relatively Fixed for a Given Process
• Larger Wafer → Lower Cost/Die
Historical Trends
Memory Density (Bits/Chip)

- Moore’s Law - Exponential Increase in Chip Complexity
- ISSCC Research Benchmarks
  - 1967 - 64 bit Memory
  - 1984 - 1Mb Memory
  - 1995 - First 1 Gb Memory

FIGURE 1.2
(a) Dynamic memory density versus year since 1960.
Historical Trends
Microprocessor Complexity (Trans./Chip)

- ISSCC Benchmarks
  - 1971 - 2000 Transistors
  - 1988 - 1M Transistors
  - 1998 - 100M Transistors

FIGURE 1.2
(b) Number of transistors in a microprocessor versus year.
Historical Trends
Memory Feature Size (μm)

- Feature Size Decreases by 2X approximately every 5 years
- Each New Process Generation Doubles Density - Reduction of Feature Size by 0.707
- The Original Nanotechnology!
  - Feature size now 70-90 nm
- Transistors Operate Normally

**FIGURE 1.3**
Feature size used in fabrication of dynamic memory as a function of time.
Semiconductor Industry Roadmap - ITRS

TABLE 1.1 International Technology Road Map for Semiconductors (ITRS) [4]

<table>
<thead>
<tr>
<th>Year of First Product Shipment</th>
<th>Selected Projections</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM Metal Line Half-Pitch (nm)</td>
<td>150</td>
</tr>
<tr>
<td>Microprocessor Gate Widths (nm)</td>
<td>100</td>
</tr>
<tr>
<td>DRAM (G-bits/chip)</td>
<td>2.2</td>
</tr>
<tr>
<td>Microprocessor (M-transistors/chip)</td>
<td>48</td>
</tr>
<tr>
<td>DRAM Chip Area: Year of Introduction (mm²)</td>
<td>400</td>
</tr>
<tr>
<td>DRAM Chip Area: Production (mm²)</td>
<td>130</td>
</tr>
<tr>
<td>MPU Chip Size at Introduction (mm²)</td>
<td>340</td>
</tr>
<tr>
<td>MPU Chip Area: Second “shrink” (mm²)</td>
<td>180</td>
</tr>
<tr>
<td>Wafer Size (mm)</td>
<td>300</td>
</tr>
</tbody>
</table>


Each new process generation doubles chip density by scaling feature size by 0.7.
NMOS Transistor
Top View and Cross-Section

- **N-Channel Metal-Oxide Semiconductor Transistor**
- **n- and p-type semiconductor regions**
- **Thick and thin oxides**
- **Etching Openings**
- **Polysilicon gate**
- **Metal (Al) Interconnections**

*FIGURE 1.4*
The basic structure of an n-channel metal-oxide-semiconductor (NMOS) transistor structure. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a). The transistor uses heavily doped polysilicon as the gate “metal.”
Basic NMOS Process

Key Steps

- Oxidation
- Photolithography
- Implantation
- Diffusion
- Etching
- Film Deposition

**FIGURE 1.6**
Process sequence for a semirecessed oxide NMOS process. (a) Silicon wafer covered with silicon nitride over a thin padding layer of silicon dioxide; (b) etched wafer after first mask step. A boron implant is used to help control field oxide threshold; (c) structure following oxidation, nitride removal, and polysilicon deposition; (d) wafer after second mask step and etching of polysilicon; (e) the third mask has been used to open contact windows following silicon dioxide deposition; (f) final structure following metal deposition and patterning with fourth mask.

Cross-section view

- Silicon nitride
- SiO₂
- p-type silicon
- Boron implant
- Polysilicon
- Phosphorus or arsenic
- CVD SiO₂
- SiO₂
- Al
- CVD polysilicon deposition

Top view of masks

- Thermal oxidation
- CVD nitride deposition
- Active area mask
- Boron field implant
- Thermal field oxidation
- Remove nitride and oxide pad
- Regrow thin gate oxide
- Boron threshold-adjustment implant
- CVD oxide deposition
- Source/drain implantation
- Source/drain diffusion
- Contact openings
- Metal deposition
- Pattern metal
- Etch metal
- Passivation layer deposition
- Open bonding pads
CMOS Technology

N-Well Technology Cross-Section

- **Complementary Metal-Oxide Semiconductor Technology**
- **Dominant Technology in Integrated Circuits Today!**
- Requires both NMOS and PMOS Transistors

**Oxidation**

**Photolithography**

**Implantation**

**Diffusion**

**Etching**

**Film Deposition**

**FIGURE 1.8**

Cross-sectional views at major steps in a basic CMOS process. (a) Following n-well diffusion, (b) following selective oxidation, and (c) following gate oxidation and polysilicon gate definition; (d) NMOS source/drain implantation; (e) PMOS source/drain implantation; (f) structure following contact and metal mask steps.
Bipolar Transistor
Top View and Cross-Section

- Bipolar Junction Transistor (BJT)
- Standard Buried Collector Process (SBC)
- n- and p-type semiconductor regions
- Thick and thin oxides
- Etching Openings
- Metal (Al) Interconnections

FIGURE 1.5
The basic structure of a junction-isolated bipolar transistor. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a).
SBC Process

Key Steps

- Oxidation
- Photolithography
- Implantation
- Diffusion
- Etching
- Film Deposition

**FIGURE 1.9**
Cross-sectional view of the major steps in a basic bipolar process. (a) Wafer with silicon dioxide layer; (b) following buried-layer diffusion using first mask, and subsequent epitaxial layer growth and oxidation; (c) following deep-isolation diffusion using second mask; (d) following boron-base diffusion using third mask; (e) fourth mask defines emitter and collector contact regions; (f) final structure following contact and metal mask steps.
References

[1] *Digest of the IEEE International Solid-State Circuit Conference*, held in February of each year. (http://www.sscs.org/isscc)


[3] *Digests of the International VLSI Technology and Circuits Symposia*, co-sponsored by the IEEE and JSAP, held in June of each year. (http://www.vlsisymposium.org)

End of Chapter 1