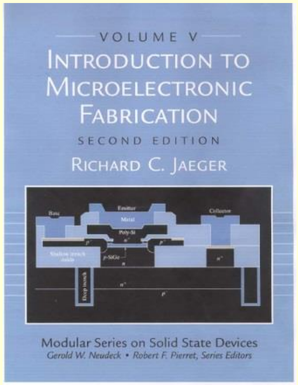
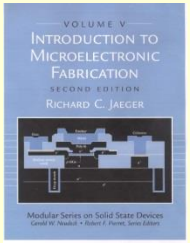
# Introduction to Microelectronic Fabrication

Chapter 6
Film Deposition



# Evaporation
## High Vacuum System



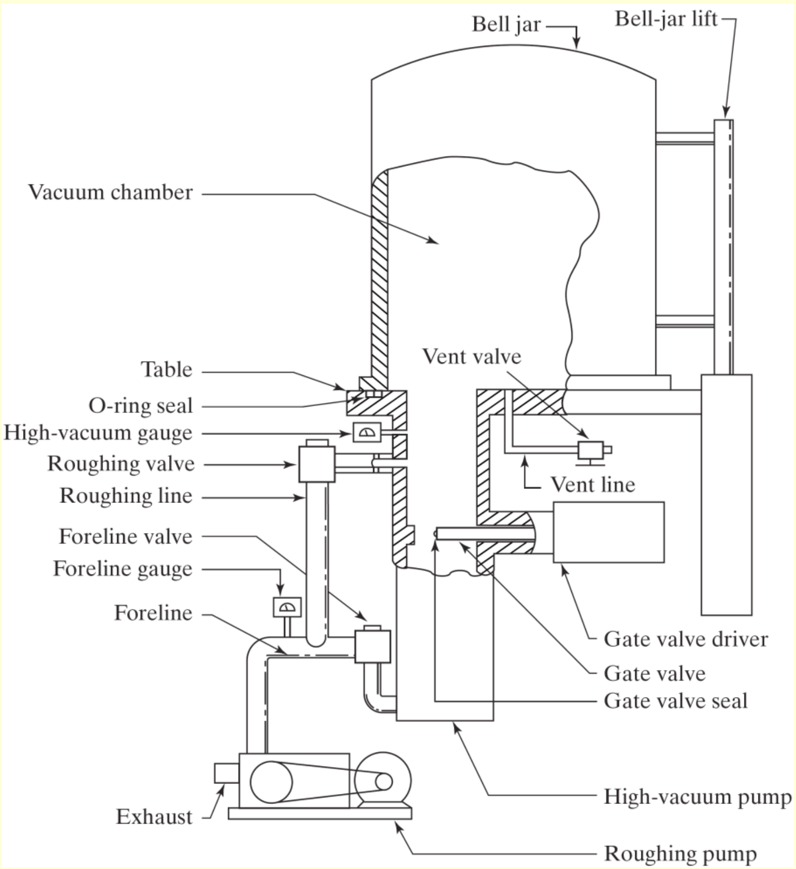
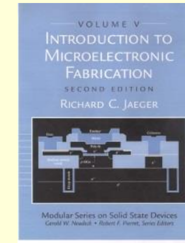
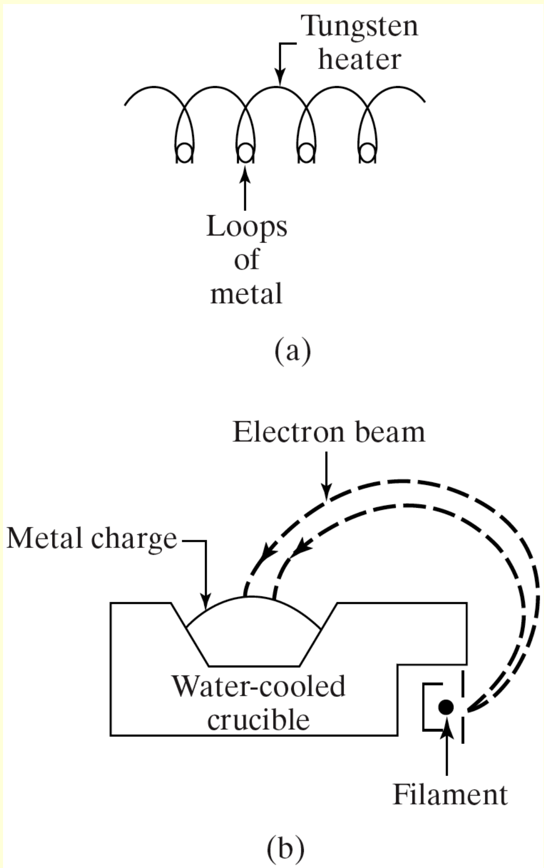




FIGURE 6.1

Typical vacuum system used for evaporation including vacuum chamber, roughing pump, high-vacuum pump, and various valves and vacuum gauges. Copyright 1987 McGraw-Hill Book Company. Reprinted with permission from Ref. [5].

# Evaporation
## Filament & Electron Beam

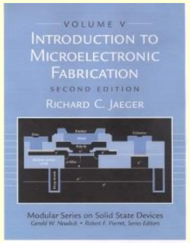



(a) Filament Evaporation with Loops of Wire Hanging from a Heated Filament (high contamination, not thick film)

(b) High Intensity Electron Beam(15keV) is Focused on Metal Charge by a Magnetic Field

# Evaporation
## Electron Beam



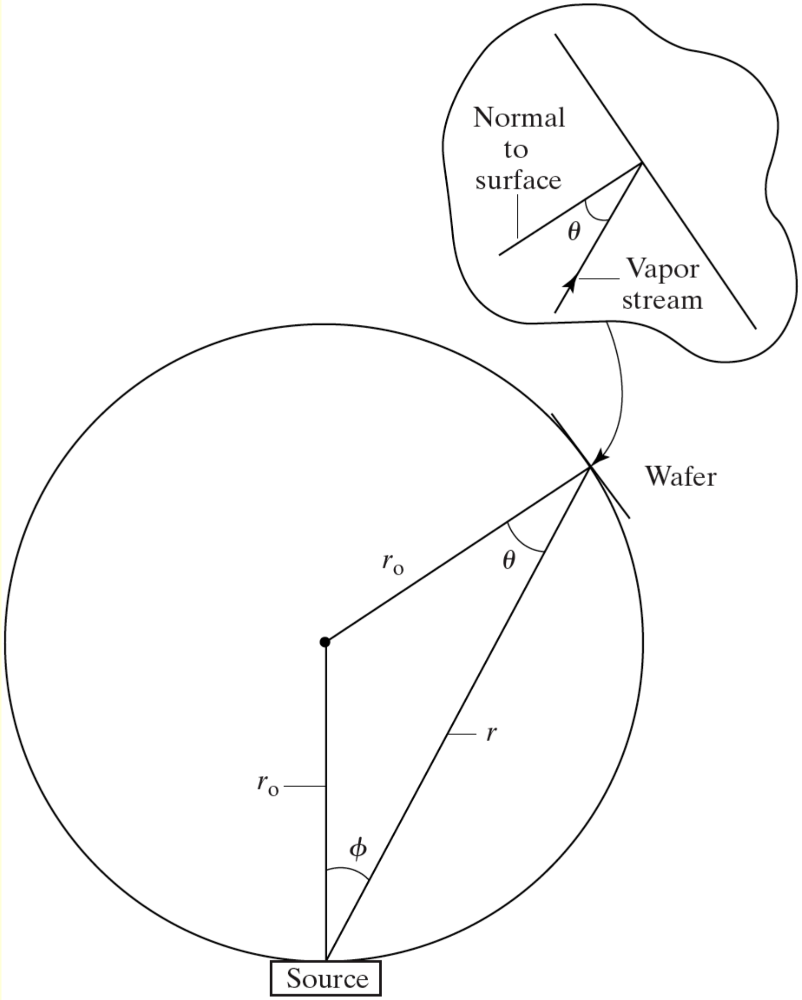




FIGURE 6.4

Photograph of a laboratory E-beam evaporation system with a planetary substrate holder which rotates simultaneously around two axes.

Growth Rate (cm/sec)

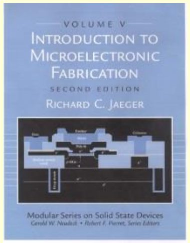
$$G = \frac{m}{\pi \rho r^2} \cos\phi \cos\theta$$

$$\cos\phi = \cos\theta = \frac{r}{2r_o}$$

$$G = \frac{m}{4\pi\rho r_o^2}$$

$m$= mass evaporation rate (g/sec)
$\rho$ = density (g/cm$^3$)

# Evaporation
## Shadowing and Step Coverage



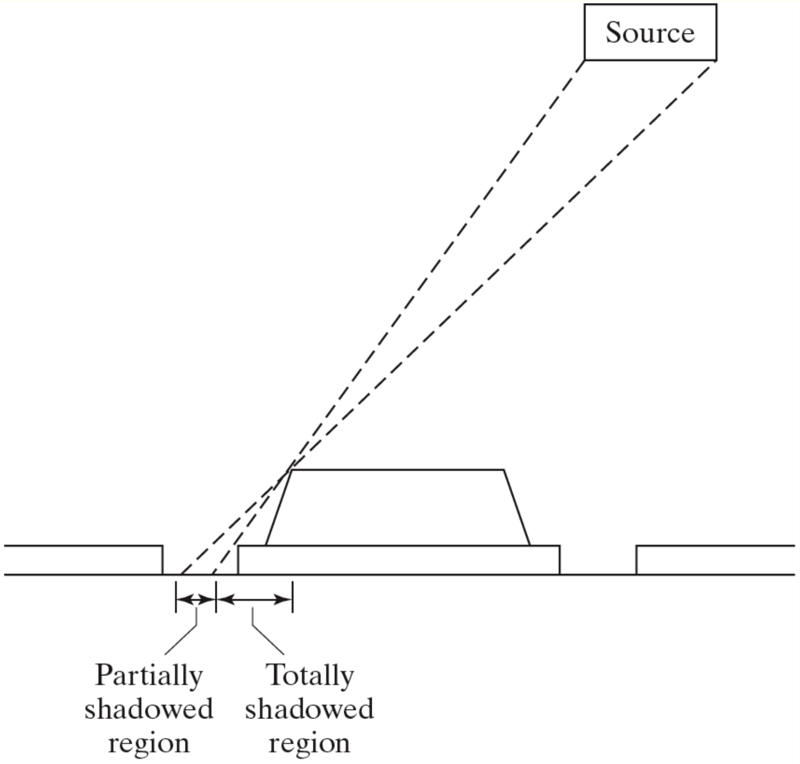




Figure 6.5

- Shadowing and Step Coverage Problems Can Occur in Low Pressure Vacuum Deposition in which the Mean Free Path is Large

Mean Free Path=average distance the molecule travels before it collides with another molecule

$$\lambda = \frac{kT}{\sqrt{2}\pi p d^2}$$

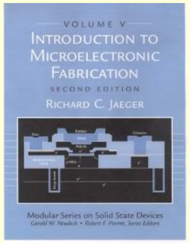
ตัวอย่าง

d=Diameter of gas molecule (2-5Å)

p=Pressure ($10^{-4}$ Pa)

ถ้า d=4Å , p= $10^{-4}$ Pa, $\lambda \approx 60$ m

# Film Deposition
# Sputtering



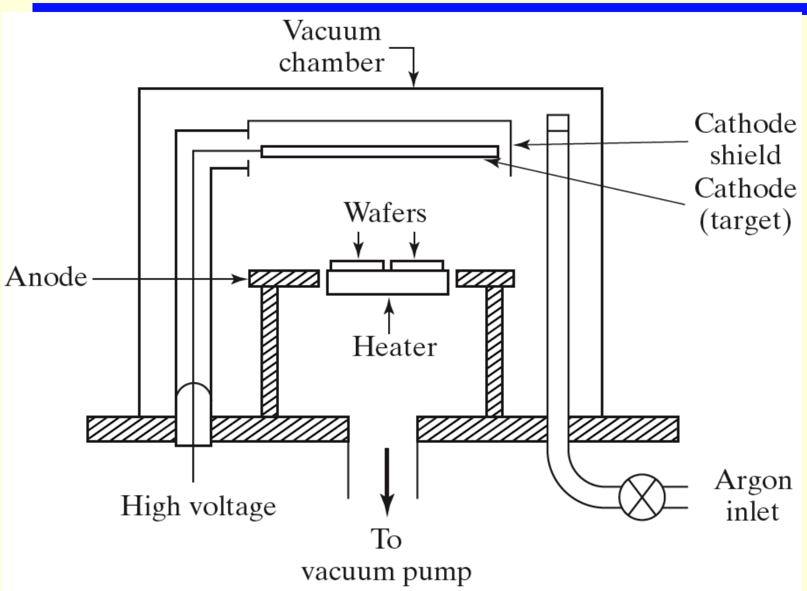




Figure 6.6
A dc sputtering system in which the target material acts as the cathode of a diode and the wafers are mounted on the system anode.

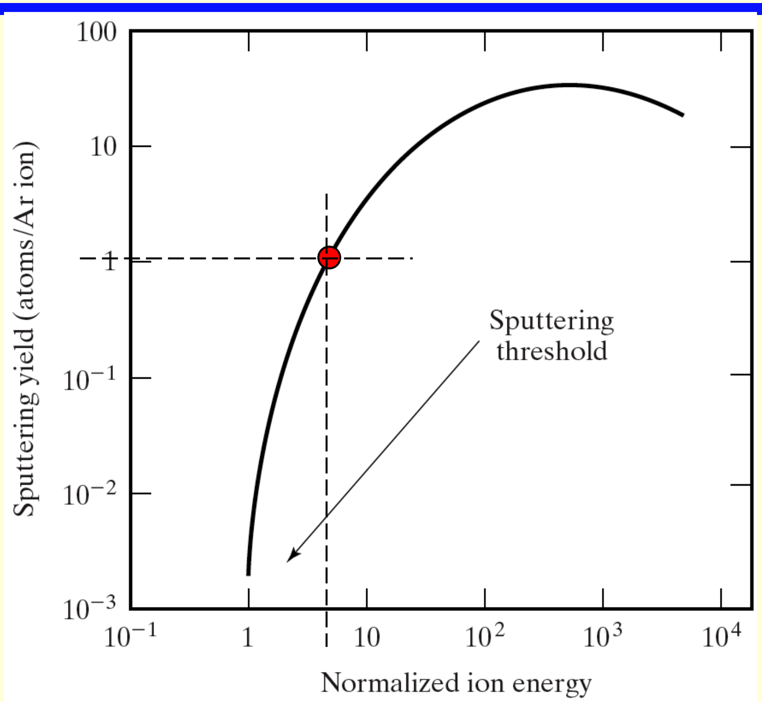



Figure 6.7
Sputtering yield increases rapidly as ion energy is increased above the sputtering threshold (argon)

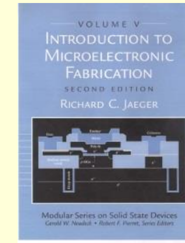
ตัวอย่าง

d=Diameter of gas molecule (2-5Å)

ถ้า d=4Å , p= 100 Pa, λ≈60 μm

$$\lambda = \frac{kT}{\sqrt{2}\pi p d^2}$$

# CVD
# Chemical Vapor Deposition




T=300-1150°C
30-250 Pa
$SiO_2$
$Si_3N_4$
PolySi

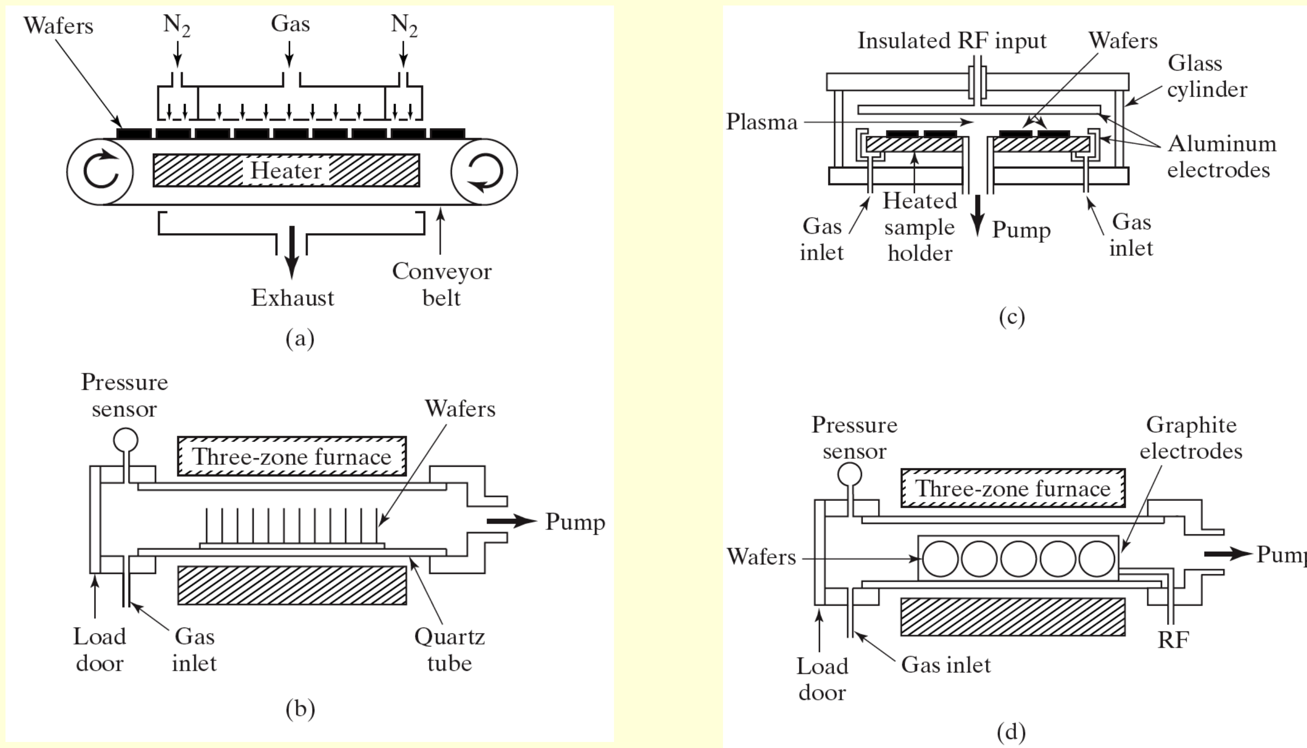
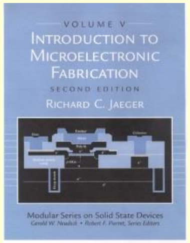



Figure 6.8
Four types of CVD systems. (a) Atmospheric-pressure reactor (b) hot-wall low-pressure (LPCVD) system in a three-zone furnace (c) parallel-plate plasma-enhanced system (d) photo-enhanced (PECVD) system using a three-zone furnace. Copyright 1983 Bell Telephone Laboratories, Inc. Reprinted with permission from Ref. [2].



For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

# CVD
## Polysilicon Deposition



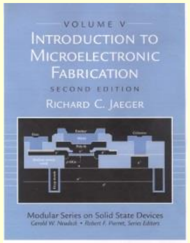

- Low Pressure Chemical Vapor Deposition (LPCVD)
  - 25-150 Pa

- Thermal Decomposition of Silane
  - 100% Silane
  - 20-30% Silane in Nitrogen

$$SiH_4 \xrightarrow{600^o C} Si + 2H_2$$

  - 100-200 Å/min at 600-650$^o$ C

# CVD
# Silicon Dioxide Deposition




Deposition of Silicon Dioxide over Aluminum (300 - 500 $C$)

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2 \qquad \mathrm{T} \leq 577^{\mathrm{o}} C(Eutectic)$$

Phosphous Doped $\mathrm{SiO}_2$ - Atmospheric Pressure or LPCVD

$$4PH_3 + 5O_2 \rightarrow 2P_2O_5 + 6H_2$$

$SiO_2$ containing 6-8% phosphorus will soften and flow at $1000\text{-}1100^{\mathrm{o}}$ C.

"P-glass reflow" can be used to smooth surface topology.

Higher Temperature Prior to Metallization

Dichlorosilane Reaction at $900^{\mathrm{o}} C$

$$SiCl_2H_2 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2HCl$$

LPCVD Decomposition of TEOS $650 - 750^{\mathrm{o}}$C

$$\mathrm{Si}(\mathrm{OC}_2H_5)_4 \rightarrow \mathrm{SiO}_2 + \mathrm{byproducts}$$



For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

# Film Deposition
## Deposited Oxide Properties

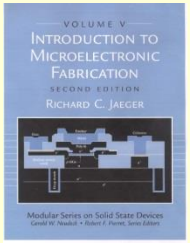
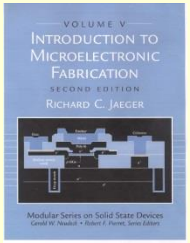



**TABLE 6.1** Properties of Various Deposited Oxides (After ref. [2])

| Source | Deposition Temperature (°C) | Composition | Conformal Step Coverage | Dielectric Strength (MV/cm) | Etch Rate (Å/min) [100:1 $H_2O$:HF] |
|---|---|---|---|---|---|
| Silane | 450 | $SiO_2$(H) | No | 8 | 60 |
| Dichlorosilane | 900 | $SiO_2$(Cl) | Yes | 10 | 30 |
| TEOS | 700 | $SiO_2$ | Yes | 10 | 30 |
| Plasma | 200 | $SiO_{1.9}$(H) | No | 5 | 400 |

# CVD
# Silicon Nitride




Silicon Nitride

- Oxidation Mask for Recessed Oxidation
- Final Passivation Layer Over Die Surface

Silane Reaction with Ammonia - $700 - 900^{\circ}C$ at Atmospheric Pressure

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$

Dichlorosilane Reaction - LPCVD at $700 - 800^{\circ}C$

$$3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2$$

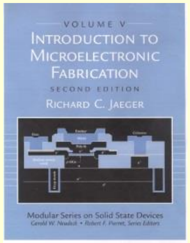
Plasma Reaction of Silane with Nitrogen

$$2SiH_4 + N_2 \rightarrow 2SiNH + 3H_2$$

Plasma Reaction of Silane with Ammonia (Argon Plasma)

$$SiH_4 + NH_3 \rightarrow SiNH + 3H_2$$

# CVD
# Metal Deposition (Mo, Ta, Ti, W)




Tungsten - Thermal, Plasma or Optical Assisted Decomposition of $WF_6$

$$WF_6 \rightarrow W + 3F_2$$

Tungsten - Reduction of $WF_6$ with Hydrogen

$$WF_6 + 3H_2 \rightarrow W + 6HF$$

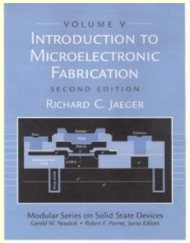
Mo, Ta and Ti - LPCVD Reaction with Hydrogen

$$2MCl_5 + 5H_2 \rightarrow 2M + 10HCl$$

––––––

Copper is Deposited by "Standard" Plating Techniques

# Film Deposition
# Epitaxial Growth




- Vapor Phase Epitaxy

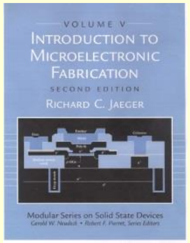
- Liquid Phase Epitaxy
  - Compound Semiconductors

- Molecular Beam Epitaxy
  - Compound Semiconductors

- III-V Compound Semiconductors
  - GaAs, InP, GaInAs, InAs …

# End of Chapter 6

# Epitaxial Growth
## Vapor Phase Epitaxy



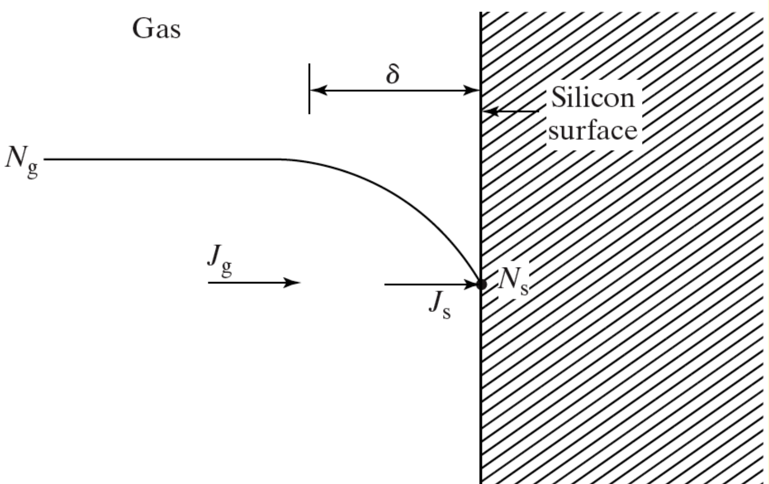




Figure 6.9

Gas diffuses from gas stream and reacts at the surface

$$J_S = k_S N_S \qquad J_g = \left(\frac{\overline{D_g}}{\delta}\right)\left(N_g - N_S\right) = h_g\left(N_g - N_S\right)$$

$$J_S = J_g$$

Growth Rate $\quad v = \frac{J_S}{N} = \frac{k_S h_g}{k_S + h_g}\frac{N_g}{N}$

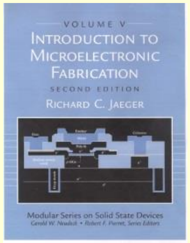
Mass Transfer Limited: $v \cong h_g \frac{N_g}{N}$ for $k_S >> h_g$

Surface Reaction Limited : $v \cong k_S \frac{N_g}{N}$ for $h_g >> k_S$




For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

# Epitaxial Growth
## Growth Rates



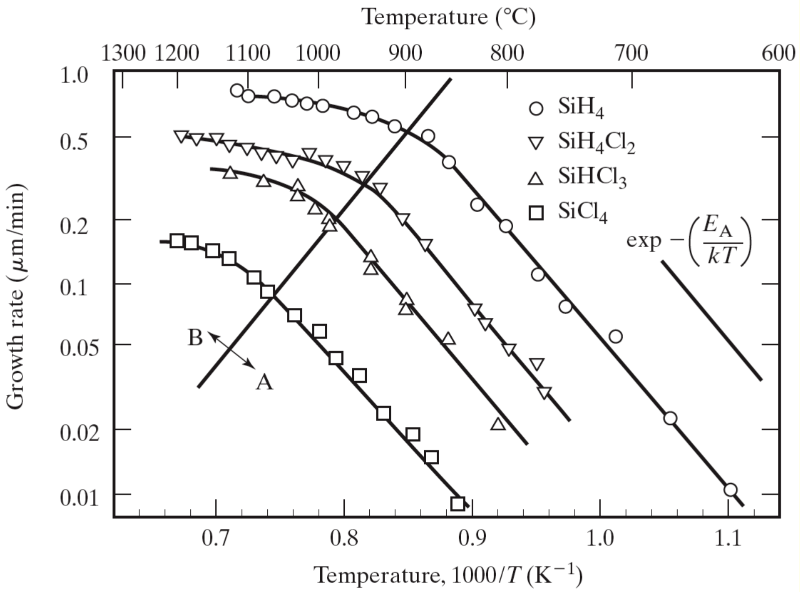




Figure 6.10
Temperature dependence of the silicon epitaxial growth process for four different sources. The growth is surface-reaction-limited in region A and is mass-transfer-limited in region B. Reprinted with permission from Philips Journal of Research from Ref. [3].

Reversible Deposition Process at 1200° C

$$SiCl_4(gas) + 2H_2(gas) \leftrightarrow Si(solid) + 4HCl(gas)$$

HCl in Input Stream can be Used to Clean Surface

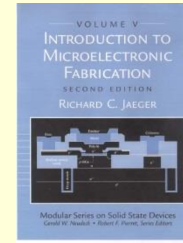
Competing Etching Reaction

$$SiCl_4(gas) + Si(solid) \leftrightarrow 2SiCl_2(gas)$$

Alternative - Pyrolytic Decomposition of Silane

$$SiH_4 \xrightarrow{600^o C} Si + 2H_2$$

# Epitaxial Growth
## Vapor Phase Systems



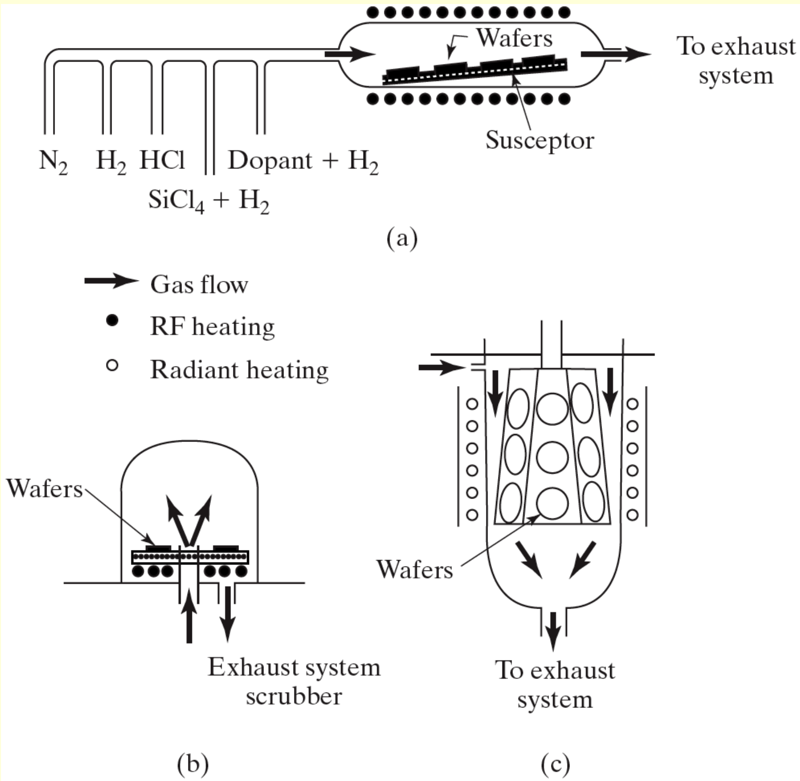
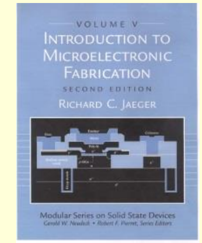
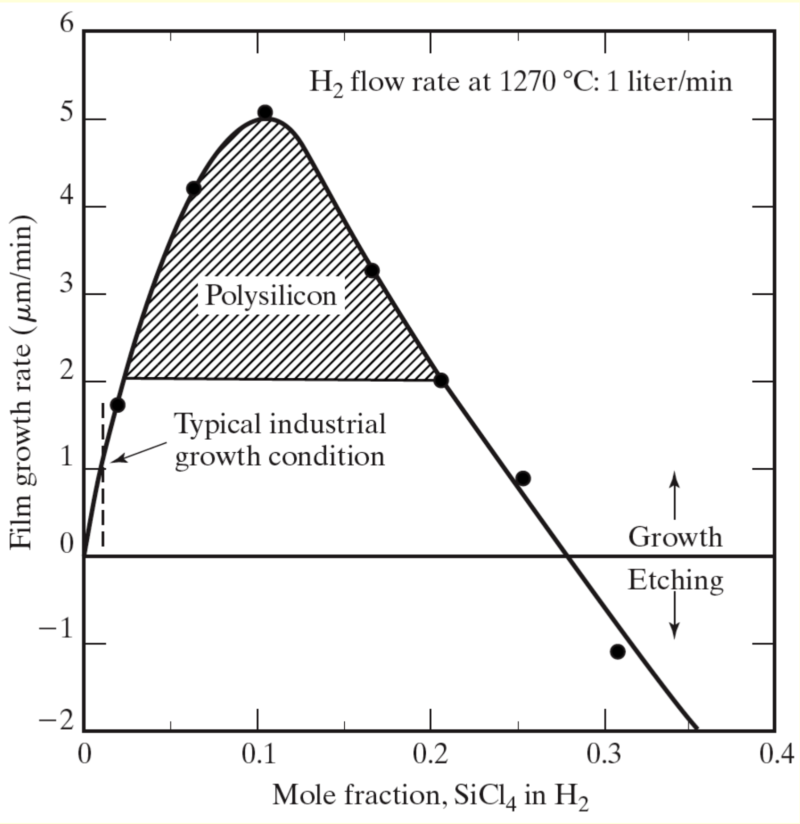




**FIGURE 6.11**

(a) Horizontal, (b) pancake, and (c) barrel susceptors commonly used for vapor-phase epitaxy. Copyright 1985 John Wiley & Sons, Inc., with permission from Ref. [1].

# Epitaxial Growth
## Growth in Silicon Tetrachloride




Single Crystal Silicon Growth for Rates Below 2 μm/min

Etching for High $SiCl_4$ Concentrations

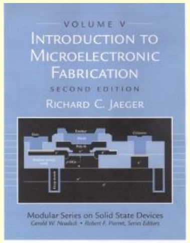
FIGURE 6.12

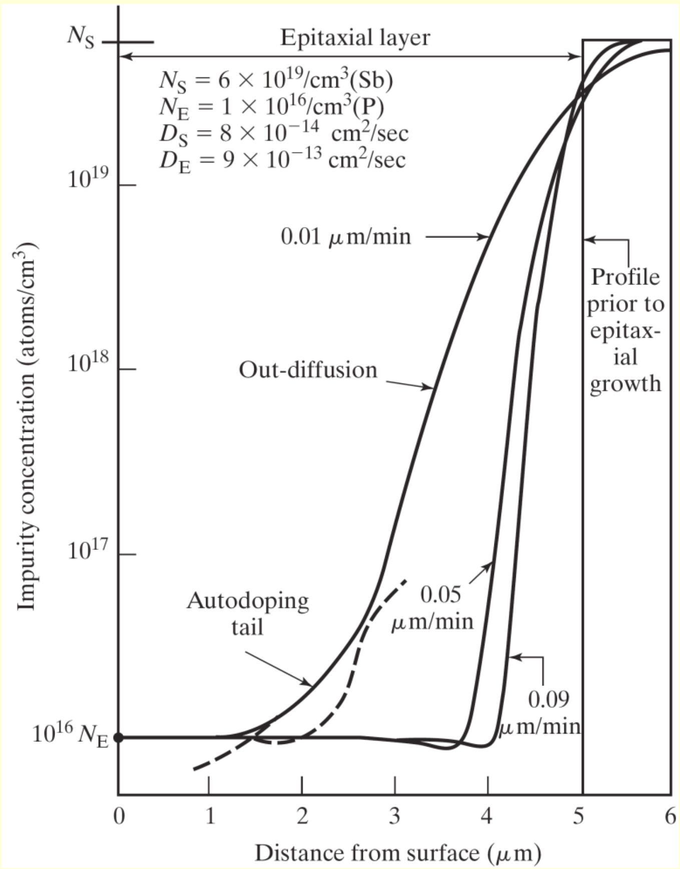
Silicon epitaxial growth rate as a function of $SiCl_4$ concentration. Polysilicon deposition occurs for growth rates exceeding 2 μm/min. Etching of the surface will occur for mole fraction concentrations exceeding 28%. Copyright 1985 John Wiley & Sons, Inc, with permission from Ref. [1].



For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

# Epitaxial Growth
## Impurity Redistribution



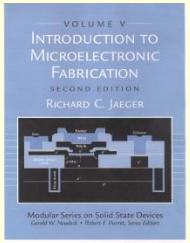

Moving Boundary Diffusion Problem

$$D\frac{\partial^2 N}{\partial x^2} = \frac{\partial N}{\partial t} + v_x \frac{\partial N}{\partial x}$$

FIGURE 6.13

Redistribution of impurity atoms due to gas-phase autodoping and impurity out-diffusion during epitaxial layer growth. Out-diffusion is calculated using eq. (6.33) for epitaxial growth of a phosphorus-doped layer at 1150 °C over an antimony-doped buried layer with a surface concentration of 6 x $10^{19}/cm^3$. The three curves are for growth rates of 0.01, 0.05, and 0.09 µm/min. For clarity, the effects of autodoping are shown on only one curve.

# Epitaxial Growth
## Geometrical Model



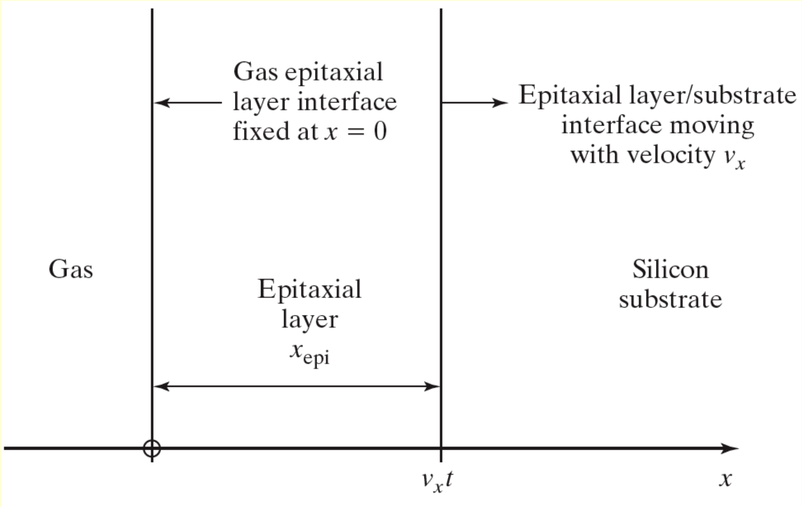




Figure 6.4

$$D\frac{\partial^2 N}{\partial x^2} = \frac{\partial N}{\partial t} + v_x \frac{\partial N}{\partial x}$$

Solution is Superposition of Two Cases

$$N(x,t) = N_1(x,t) + N_2(x,t)$$

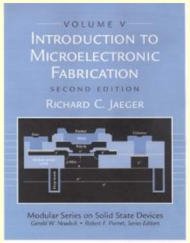
Undoped Epi-Layer on Uniformly Doped Substrate

$$N_1(x,t) = \frac{N_S}{2}\left[1 + erf\left(\frac{x - x_{epi}}{2\sqrt{D_S t}}\right)\right]$$

Doped Epi-Layer on Undoped Substrate

$$N_2(x,t) = \frac{N_E}{2}\left[1 + erfc\left(\frac{x - x_{epi}}{2\sqrt{D_E t}}\right) + \exp\frac{v_x x}{D_E} erfc\left(\frac{x + x_{epi}}{2\sqrt{D_E t}}\right)\right]$$

# Epitaxial Growth
## Pattern Shift



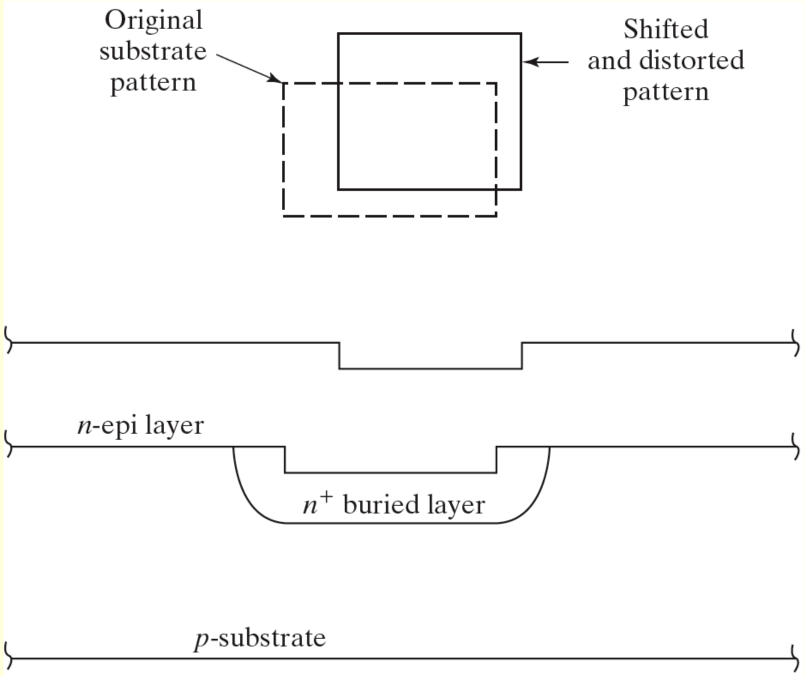



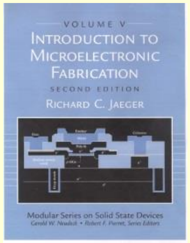

Figure 6.15

- Pattern Shift During Epitaxial Growth Over an $n^+$ Buried Layer.
- Pattern is Both Shifted and Distorted in Shape



For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

# Film Deposiiont References & Further Reading




**REFERENCES**

**[1]** S. M. Sze, *Semiconductor Devices—Physics and Technology*, John Wiley & Sons, New York, 1985.

**[2]** A. C. Adams, "Dielectric and Polysilicon Film Deposition," Chapter 3 in S. M. Sze, Ed., *VLSI Technology*, McGraw-Hill, New York, 1983.

**[3]** F. C. Eversteyn, "Chemical-Reaction Engineering in Semiconductor Industry," *Philips Research Reports, 29*, 45–66 (February, 1974).

**[4]** A. B. Glaser and G. E. Subak-Sharpe, *Integrated Circuit Engineering*, p. 205–209, Addison-Wesley, Reading, MA, 1979.

**[5]** W. S. Ruska, *Microelectronic Processing*, McGraw-Hill, New York, 1987.

**FURTHER READING**

**[1]** J. L. Vossen and W. Kern, Eds., *Thin Film Processes*, Academic Press, New York, 1978.

**[2]** J. F. O'Hanlon, *A User's Guide to Vacuum Technology*, John Wiley & Sons, New York, 1980.

**[3]** L. Holland, *Vacuum Deposition of Thin Films*, John Wiley & Sons, New York, 1961.

**[4]** A. S. Grove, *Physics and Technology of Semiconductor Devices*, John Wiley & Sons, New York, 1967.

**[5]** H. C. Theuerer, "Epitaxial Silicon Films by Hydrogen Reduction of $SiCl_4$," *Journal of the Electrochemical Society, 108*, 649–653 (July, 1961).

**[6]** C. O. Thomas, D. Kahng, and R. C. Manz, "Impurity Distribution in Epitaxial Silicon Films," *Journal of the Electrochemical Society, 109*, 1055–1061 (November, 1962).

**[7]** A. S. Grove, A. Roder, and C. T. Sah, "Impurity Distribution in Epitaxial Growth," *Journal of Applied Physics, 36*, 802–810 (March, 1965).

**[8]** D. Kahng, C. O. Thomas, and R. C. Manz, "Epitaxial Silicon Junctions," *Journal of the Electrochemical Society, 110*, 394–400 (May, 1963).

**[9]** W. H. Shepherd, "Vapor Phase Deposition and Etching of Silicon," *Journal of the Electrochemical Society, 112*, 988–994 (October, 1965).

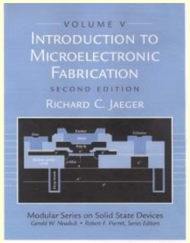
**[10]** G. R. Srinivasan, "Autodoping Effects in Silicon Epitaxy," *Journal of the Electrochemical Society, 127*, 1334–1342 (June, 1980).

**[11]** J. C. Bean, "Silicon Molecular Beam Epitaxy as a VLSI Processing Technique," 1981 *IEEE IEDM Proceedings*, p. 6–13.



For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

# Copyright Notice






© 2002 Pearson Education, Inc., Upper Saddle River, NJ. All rights reserved. This material is protected under all copyright laws as they currently exist. No portion of this material may be reproduced, in any form or by any means, without permission in writing from the publisher.

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

# End of Chapter 6



For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.